Model Name: SOM-DB5830

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Title: COVER		
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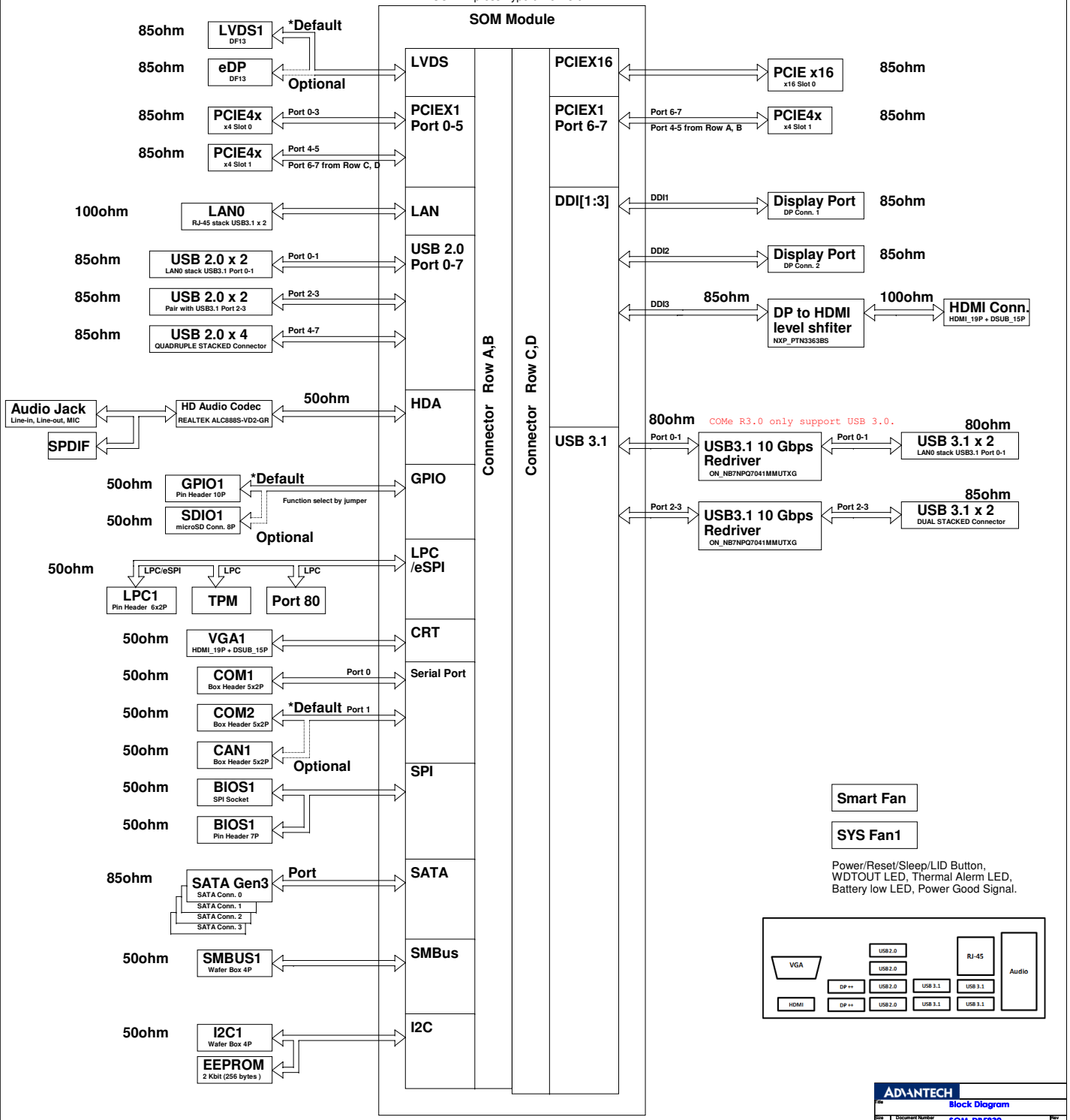
COM-Express Type 6 Rev. 3.0



Smart Fan

SYS Fan1

Power/Reset/Sleep/LID Button,
WDTOUT LED, Thermal Alerm LED,
Battery low LED, Power Good Signal.

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Title: Block Diagram

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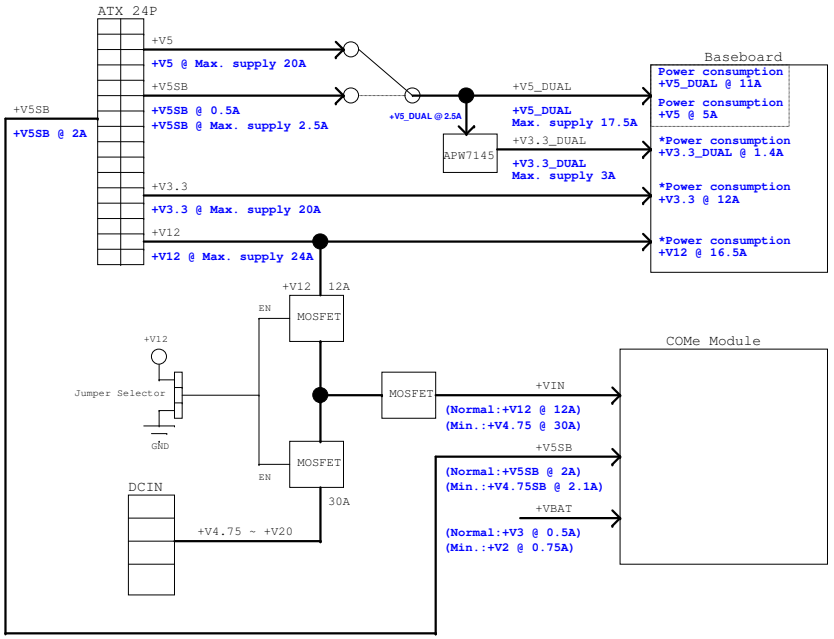

Table 57: PCIe Connector Power and Bulk Decoupling Requirements

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector
VCC_12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk
VCC_3V3	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk
VCC_3V3_SB	375mA @ 150uF bulk	375mA @ 150uF bulk

Table 7.2: Input Power - Pin-Out Type 6/7 Modules (Dual Connector, 440 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/-100	137	85%	116
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2 0 - 3.3		+/-20			

ATX12V Power Supply Design Guide

Table 4. Typical Power Distribution for a 300 W ATX12V Configuration

Output	Min. Current (amps)	Max. Current (amps)	Peak Current (amps)
+12 V1DC[1, 2]	1.0	8.0	10.0
+12 V2DC[1, 2]	1.0	14.0	
+5 VDC	0.3	20.0	
+3.3 VDC	0.5	20.0	
-12 VDC	0.0	0.3	
+5 VSB	0.0	2.0	2.5

Note: Total combined output of 3.3 V and 5 V is ≤ 120 W
Peak currents may last up to 17 seconds with not more than one occurrence per minute
[1]12V1DC and 12V2DC should have separate current limit circuits to meet 240VA safety requirements.
[2]12V2 supports processor power requirements and must have a separate current limit

LVDS PWR

+V12	+V12 +VLVDS_PANEL_PWR	1A (40mils)
+V5	+V5 +VLVDS_PANEL_PWR	1A (40mils)
+V3.3	+V3.3 +VLVDS_PANEL_PWR	1A (40mils)

System FAN / Smart FAN

+V12	2.2 x2 = 4.4A	4.4A (176mils)

PCIE Slot

+V12	+V12 PCIe X16 x1 + PCIe X4 x2 5.5A + (2.1A x2) = 9.7A (388mils)	
+V3.3	+V3.3 PCIe X16 x1 + PCIe X4 x2 3A + (3A x2) = 9A (360mils)	
+V3.3_DUAL	+V3.3_DUAL PCIe X16 x1 + PCIe X4 x2 375mA + (375mA x2) = 1125mA (45mils)	

BUZZER

+V5	+V5	50mA (2mils)

ON_NCP45521IMNTWG-H

+V3.3	+V3.3	1A (40mils)
+V3.3_SDIO	+V3.3_SDIO	1A (40mils)

VGA

+V5	+V5	1A (40mils)

ANPEC_APW7145KAI-TRG

+V5_DUAL	+V5_DUAL	2.5A (100mils)
+V3.3_DUAL	+V3.3_DUAL	3 A (120mils)

REALTEK_ALC888S-VD2-GR

+V3.3	+V3.3	20.47mA (0.82mils)
+V5_DUAL	+V5_DUAL	237mA (10mils)

USB3.0 x 4 port

+V5_DUAL	+V5_DUAL 900mA x4 = 3.6A (144mils)	

USB2.0 x 8 port

+V5_DUAL	+V5_DUAL 500mA x8 = 4A (160mils)	

PCIE Clock Buffer

+V3.3	+V3.3 200mA (8mils)	

SN65HVD251DR

+V5	+V5	65mA (2.6mils)

ON_NB7NPQ7041MMUTXG

+V3.3_DUAL	+V3.3_DUAL 130mA x2 = 260mA (10.4mils)	

LVDS INVERTER

+V5	+V5	1A (40mils)
+V12	+V12	1A (40mils)

TPM

+V3.3_DUAL	+V3.3_DUAL	25mA (1mils)

SMBUS Pin Header

+V3.3_DUAL	+V3.3_DUAL(pin Header)	80mA (3.2mils)

I2C Pin Header + ST_M24C02-RMN6TP

+V3.3_DUAL	+V3.3_DUAL(pin Header)	82mA (4mils)

(From Module) SPI Flash + Pin Header

+V3.3_DUAL	+V3.3_DUAL	100mA (4mils)

HDMI LS

+V3.3	+V3.3	22mA (0.88mils)

HDMI Connector

+V5	+V5	55mA (2.2mils)

DP Connector x2

+V3.3	+V3.3 500mA x2 = 1A (40mils)	

LC4032V

+V3.3	+V3.3	11.8mA (0.5mils)

SP3243EUEY-L

+V5	+V5	100mA (4mils)

ATX Connector

+V12	+V12	24A (960mils)
+V3.3	+V3.3	20A (800mils)
+V5	+V5	15A (600mils)
+V5SB	+V5SB	2.5A (100mils)

ICS_ICS9112-16

+V3.3	+V3.3	40 mA (1.6 mils)

LATTICE_LC4032V-75T44C

+V3.3	+V3.3	11.8mA (0.472mils)

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Title: Power Map

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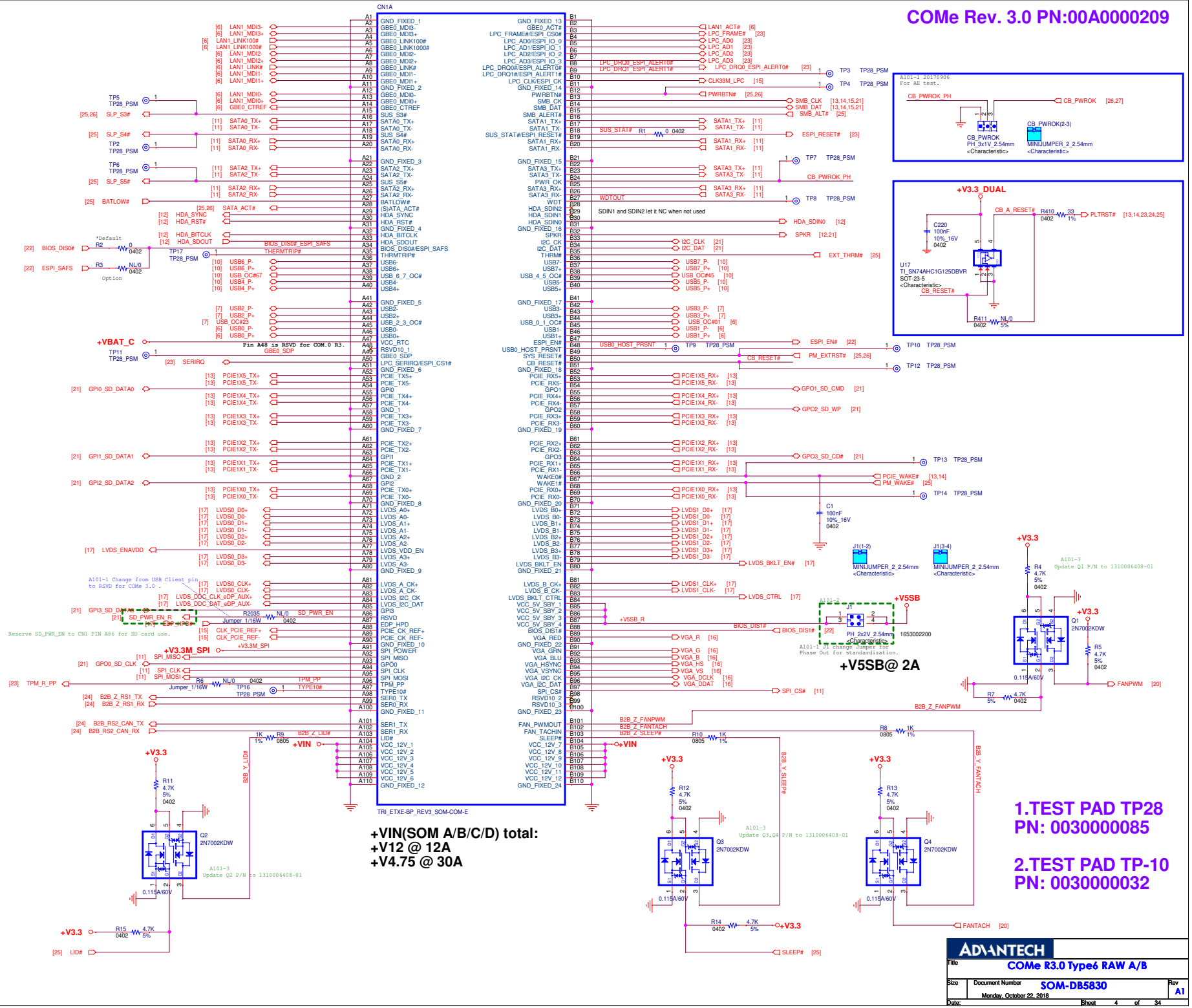
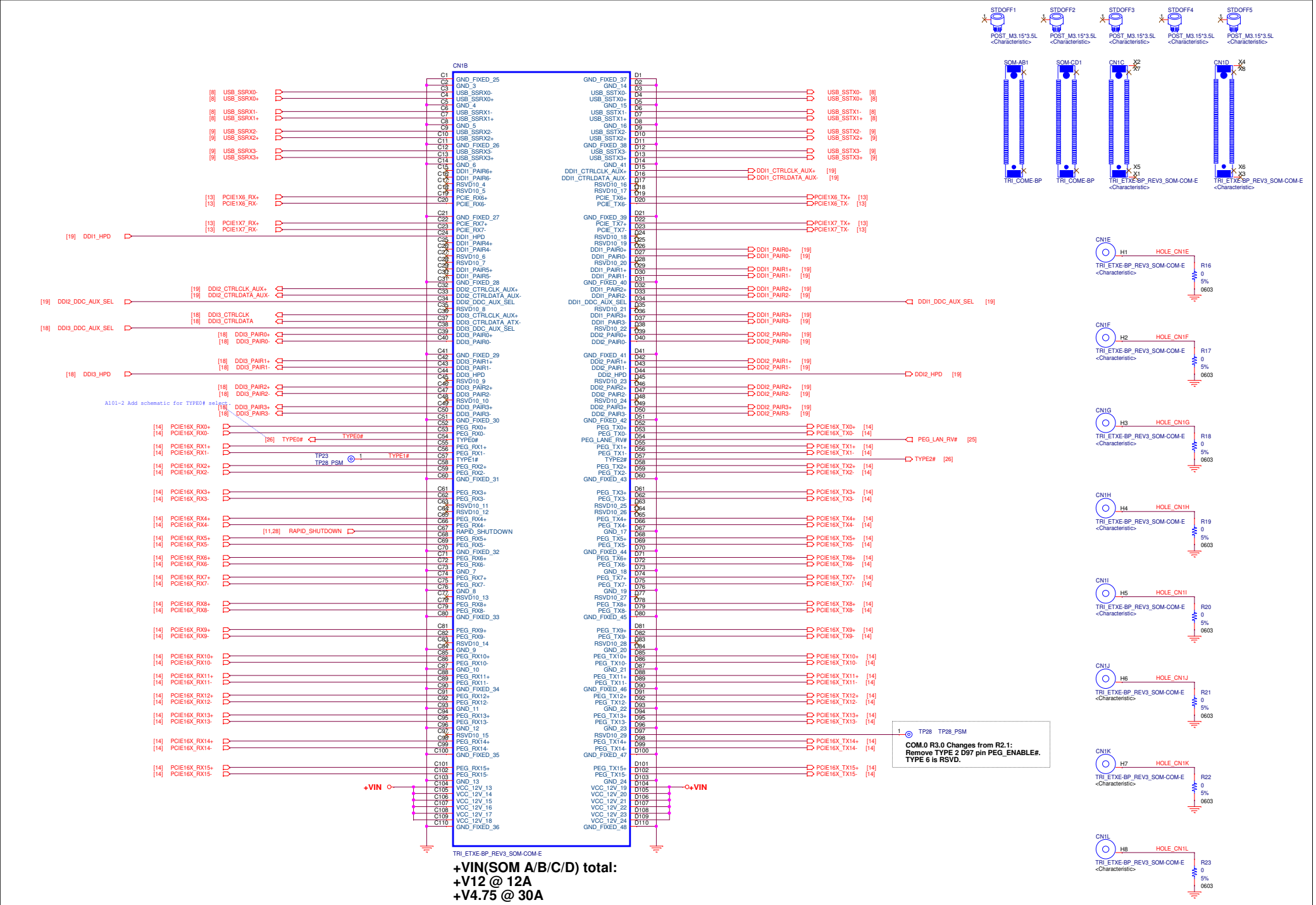
COMe Rev. 3.0 PN:00A0000209




CN1B
TRI_ETXE-BP_REV3_SOM-COM-E
+VIN(SOM A/B/C/D) total:
+V12 @ 12A
+V4.75 @ 30A
COM.0 R3.0 Changes from R2.1:
Remove TYPE 2 D97 pin PEG_ENABLE#.
TYPE 6 is RSVD.
STDOFF1
STDOFF2
STDOFF3
STDOFF4
STDOFF5
POST_M3.15*3.5L
SOM-AB1
SOM-CD1
CN1C
CN1D
TRI_COME-BP
TRI_ETXE-BP_REV3_SOM-COM-E
CN1E
CN1F
CN1G
CN1H
CN1I
CN1J
CN1K
CN1L
HOLE_CN1E
HOLE_CN1F
HOLE_CN1G
HOLE_CN1H
HOLE_CN1I
HOLE_CN1J
HOLE_CN1K
HOLE_CN1L
R16
R17
R18
R19
R20
R21
R22
R23
0603
ADVANTECH
Title
COMe R2.0 Type6 RAW C/D
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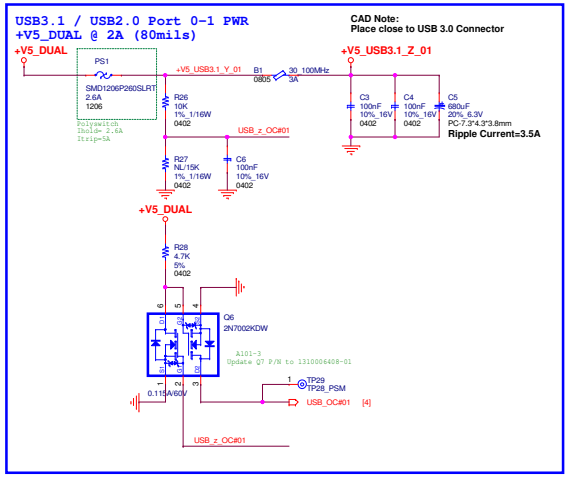
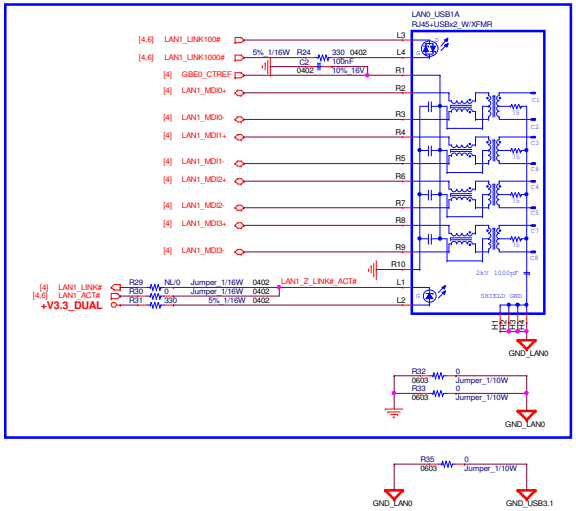
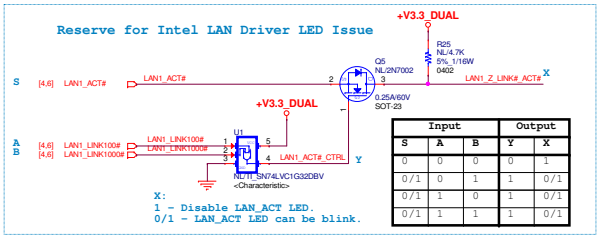
LAN0
RJ-45 (w/ USB3.1 x2)

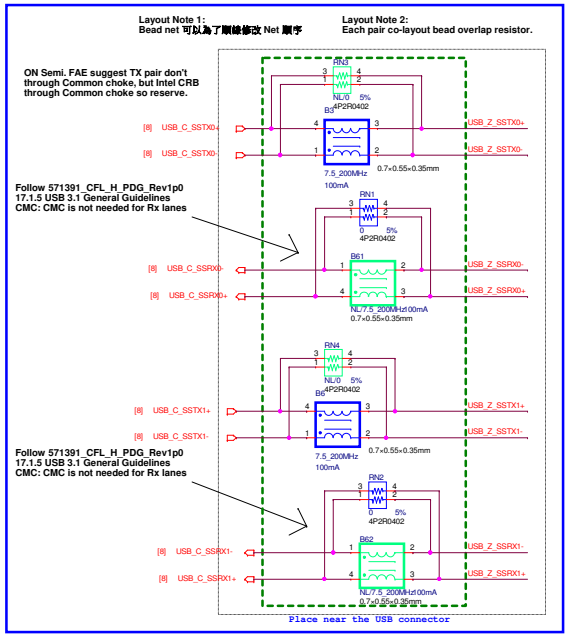


LAN0

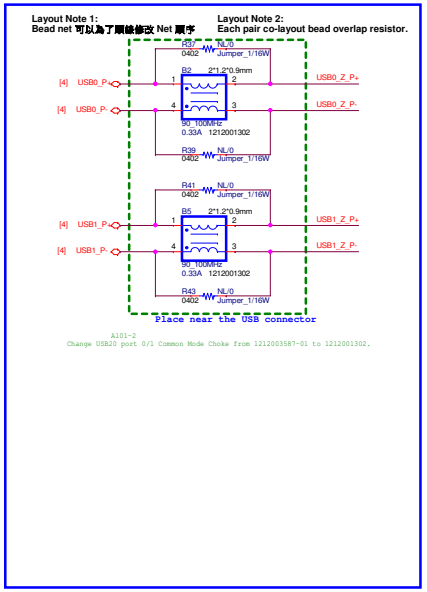




LED-Function	LED Color#	LED State	Description
Link Speed	Greed / Orange	Off	10 Mbps link speed
		Green	100 Mbps link speed
		Orange	1000 Mbps link speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, no activity detected
		Blinking	Link established, activity detected

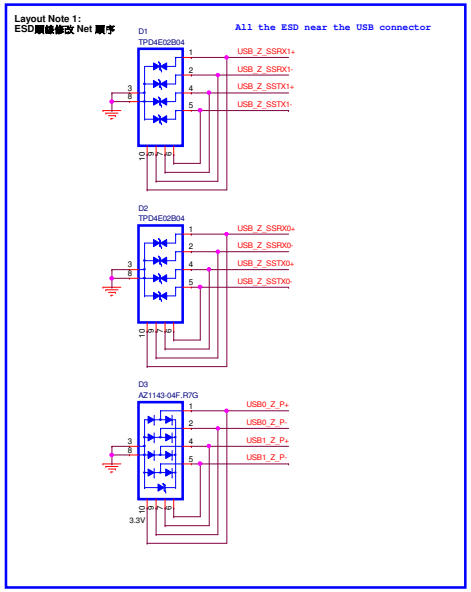


A101-2
Reserve Common Mode Choke co-layout for USB3.1 RX Port0/1 signal.

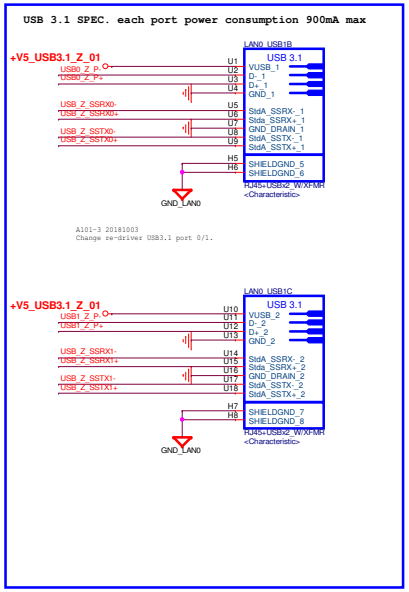


A101-2
Change USB20 port 0/1 Common Mode Choke from 1212003587-01 to 1212001302.

A101-1 170915
After ON Semi. review, ESD should work OK, but will limit bandwidth due to loss.



USB3.1 Gen2 / USB2.0



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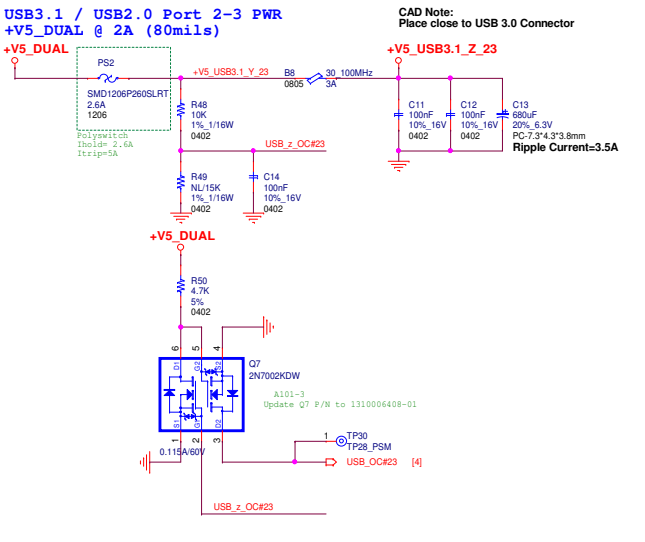
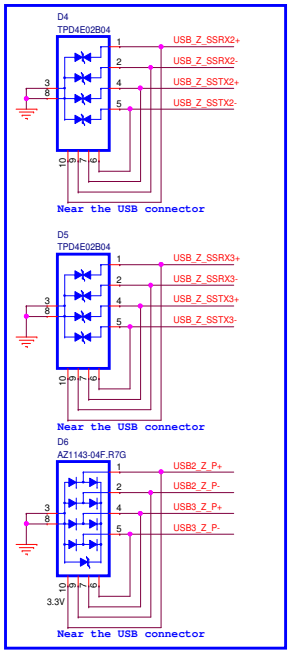
USB3.1 x2

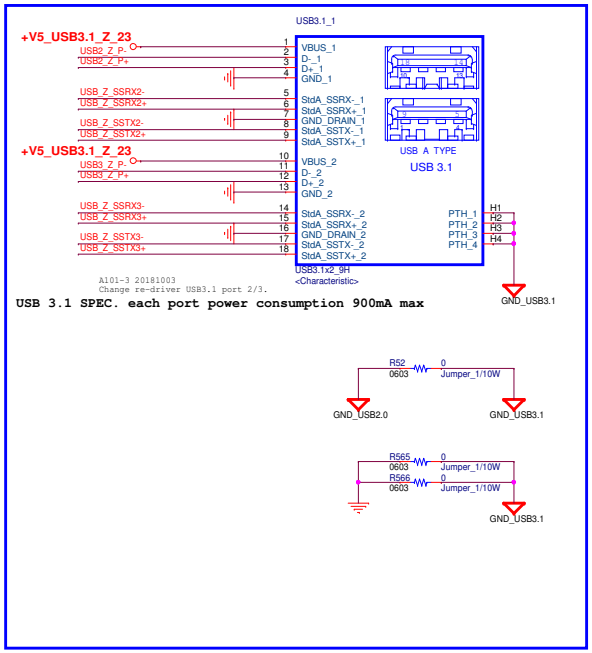


A101-1 170915
After ON Semi. review, ESD should work OK, but will limit bandwidth due to loss.

Layout Note:
ESD net 可以為了順線修改 Net 順序

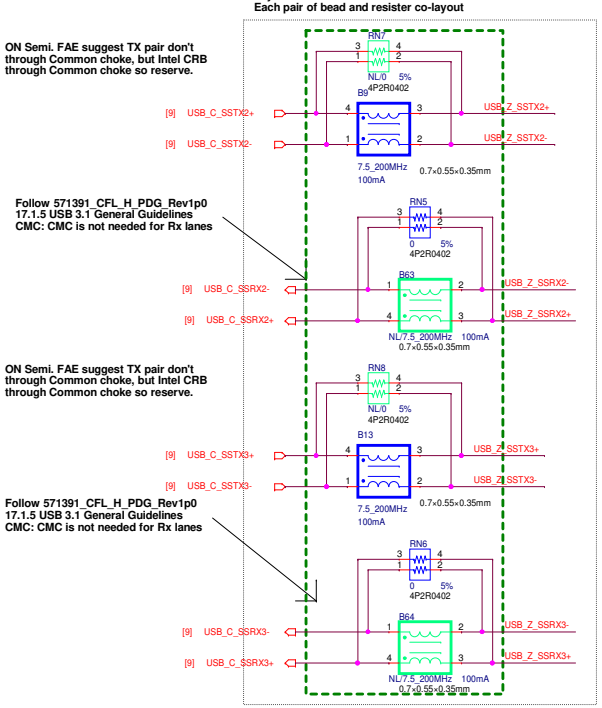


USB3.1 Connector Port 2-3



Layout Note:
Bead net 可以為了順線修改 Net 順序

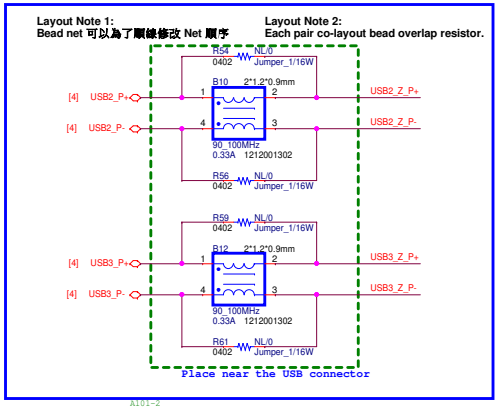
Layout Note:
Each pair of bead and resister co-layout



A101-2
Reserve Common Mode Choke co-layout for USB3.1 RX Port2/3 signal.

Layout Note 1:
Bead net 可以為了順線修改 Net 順序

Layout Note 2:
Each pair co-layout bead overlap resistor.



A101-2
Change USB20 port 2/3 Common Mode Choke from 1212003587-01 to 1212001302.

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Title	USB3.1 Port 2-3	
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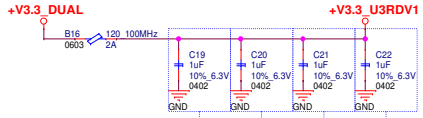
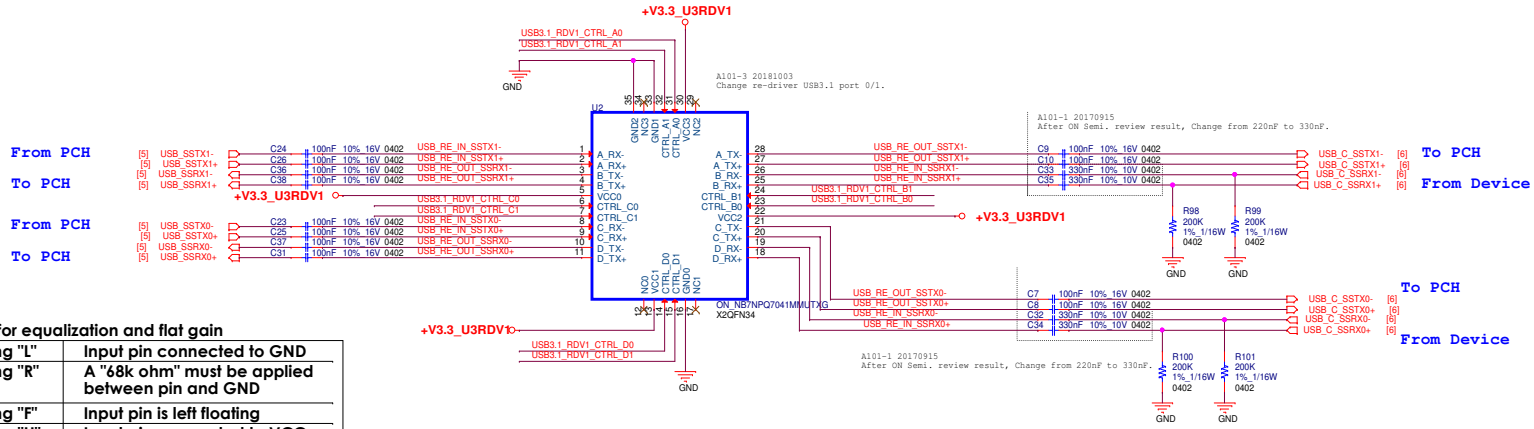
USB3.1 Gen2 Redriver for RJ45 + USB3.1 x2 Port 0-1

+V3.3_U3RDV1 @ 130mA (10.4mils)



close to pin 30
close to pin 5

close to pin 13
close to pin 22



HW Strap table for equalization and flat gain

DC Input Setting "L"	Input pin connected to GND
DC Input Setting "R"	A "68k ohm" must be applied between pin and GND
DC Input Setting "F"	Input pin is left floating
DC Input Setting "H"	Input pin connected to VCC

ON_NB7NPQ7041MMUTXG CAD Note:
Internal pull-up 100k ohm and pull-down 200k ohm.

Layout note:
Resistors place together
May 3 PADs sharing

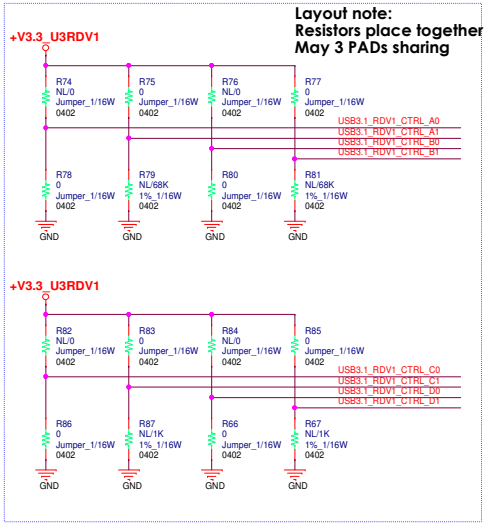


Table 2. CONTROL PIN EFFECTS (Typical Values)

Setting #	Channel A Channel C		Channel B Channel D		EQ Equalization (dB)	FG Flat Gain (dB)
	CTRL_A1 / C1	CTRL_A0 / C0	CTRL_B1 / D1	CTRL_B0 / D0		
1	L	L	L	L	5	0
2	L	R	L	R	7	0
3	L	F	L	F	8	0
4	L	H	L	H	9	0
5	R	L	R	L	10	0
6	R	R	R	R	3	2
7	R	F	R	F	4	2
8	R	H	R	H	5	2
9	F	L	F	L	7	2
10	F	R	F	R	8	2
11 (Default)	F	F	F	F	8	-1
12	F	H	F	H	5	-1
13	H	L	H	L	7	-1
14	H	R	H	R	9	-1
15	H	F	H	F	11	-1
16	H	H	H	H	7	-1

CH A
CH B
CH C
CH D

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS 4−State LVCMOS Inputs (CTRL_A0, CTRL_A1, CTRL_B0, CTRL_B1)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IL}	DC Input Setting "L"	Input pin connected to GND		GND		V
V_{IR}	DC Input Setting "R"	A specified resistor must be applied between pin and GND		0.33*V_{CC}		V
V_{IF}	DC Input Setting "F"	Input pin is left floating		0.66*V_{CC}		V
V_{IH}	DC Input Setting "H"	Input pin connected to V_{CC}		V_{CC}		V
R_{PU}	Internal pull−up resistance			100		kΩ
R_{PD}	Internal pull−down resistance			200		kΩ
R_{ext}	External Resistor for input setting "R"			68		kΩ

TYPICAL APPLICATION

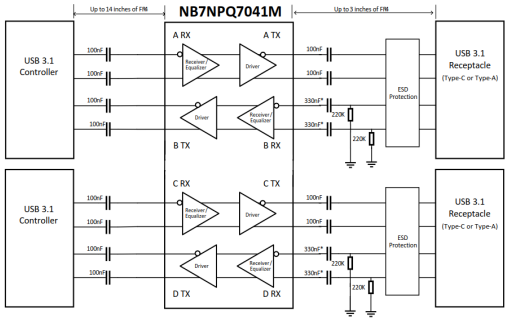


Figure 5. USB 3.1 Host Side NB7NPQ7041M Typical Application
*330nF capacitors on B RX and D RX are recommended, but not necessary in all cases.

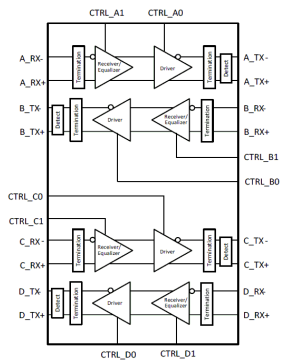


Figure 1. Logic Diagram of NB7NPQ7041M

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Title	USB3.1 Redriver Port 0-1	
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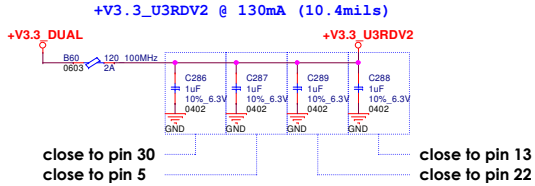
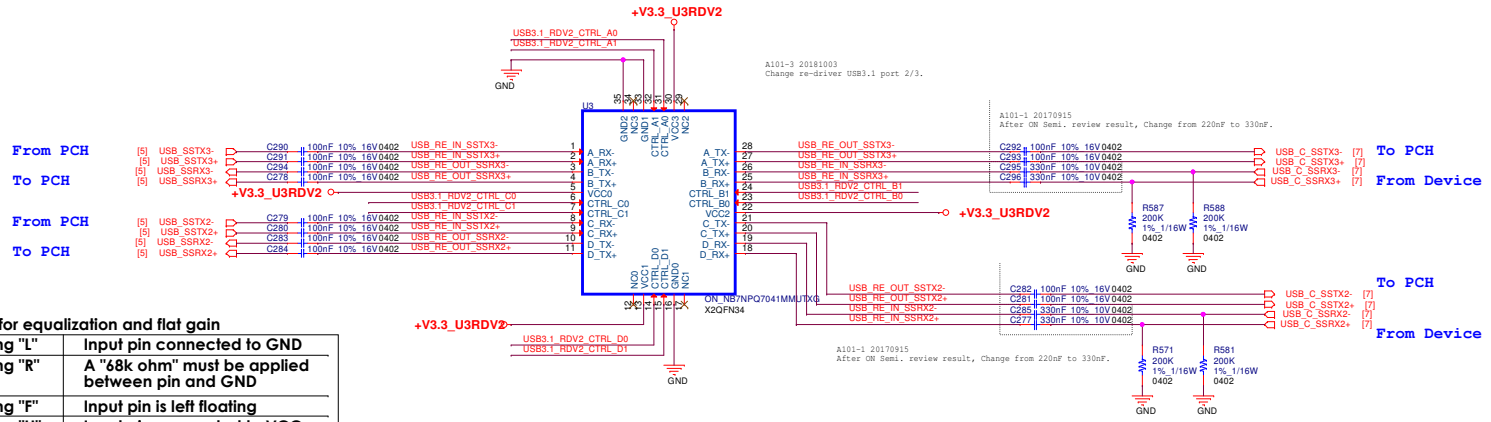
USB3.1 Gen2 Redriver for USB3.1 x2 Port 2-3





HW Strap table for equalization and flat gain

DC Input Setting "L"	Input pin connected to GND
DC Input Setting "R"	A "68k ohm" must be applied between pin and GND
DC Input Setting "F"	Input pin is left floating
DC Input Setting "H"	Input pin connected to VCC

ON_NB7NPQ7041MMUTXG CAD Note:
Internal pull-up 100k ohm and pull-down 200k ohm.

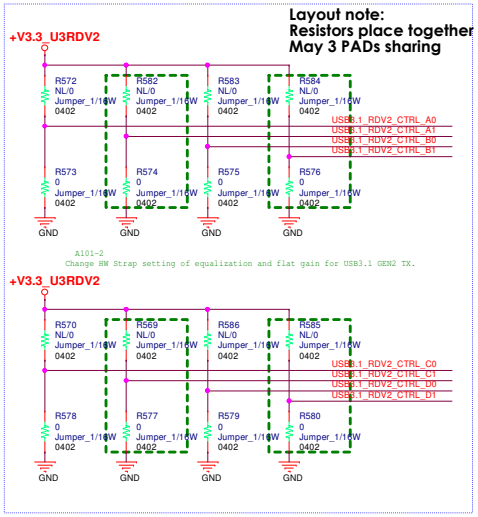


Table 2. CONTROL PIN EFFECTS (Typical Values)

Setting #	Channel A Channel C		Channel B Channel D		EQ Equalize	FG Flat Gain
	CTRL_A1 / C1	CTRL_A0 / C0	CTRL_B1 / D1	CTRL_B0 / D0		
1	L	L	L	L	4 dB	-1 dB
2	L	R	L	R	5 dB	-1 dB
3	L	F	L	F	6 dB	-1 dB
4	L	H	L	H	8 dB	-1 dB
5	R	L	R	L	9 dB	-1 dB
6	R	R	R	R	3 dB	1 dB
7	R	F	R	F	4 dB	1 dB
8	R	H	R	H	5 dB	1 dB
9	F	L	F	L	6 dB	1 dB
10	F	R	F	R	7 dB	1 dB
11 (Default)	F	F	F	F	8 dB	-2 dB
12	F	H	F	H	5 dB	-2 dB
13	H	L	H	L	7 dB	-2 dB
14	H	R	H	R	9 dB	-2 dB
15	H	F	H	F	10 dB	-2 dB
16	H	H	H	H	7 dB	-2 dB

CHA
CHB
CHC
CHD

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS 4-State LVCMOS Inputs (CTRL_A0, CTRL_A1, CTRL_B0, CTRL_B1)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IL}	DC Input Setting "L"	Input pin connected to GND		GND		V
V_{IR}	DC Input Setting "R"	A specified resistor must be applied between pin and GND		0.33*V_{CC}		V
V_{IF}	DC Input Setting "F"	Input pin is left floating		0.66*V_{CC}		V
V_{IH}	DC Input Setting "H"	Input pin connected to V_{CC}		V_{CC}		V
R_{PU}	Internal pull-up resistance			100		kΩ
R_{PD}	Internal pull-down resistance			200		kΩ
R_{ext}	External Resistor for input setting "R"			68		kΩ

TYPICAL APPLICATION

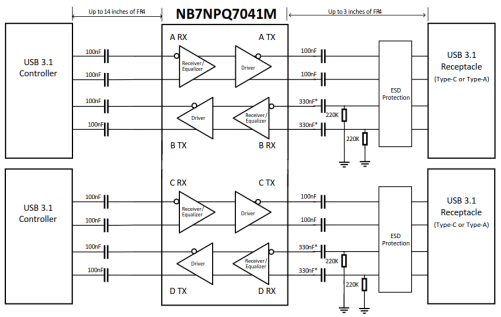


Figure 5. USB 3.1 Host Side NB7NPQ7041M Typical Application
*330nF capacitors on B RX and D RX are recommended, but not necessary in all cases.

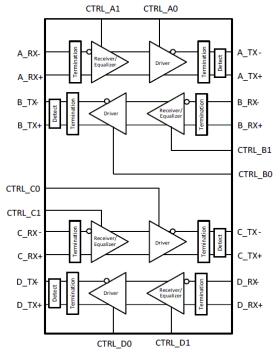


Figure 1. Logic Diagram of NB7NPQ7041M

ADVANTECH

Title	USB3.1 Redriver Port 2-3	
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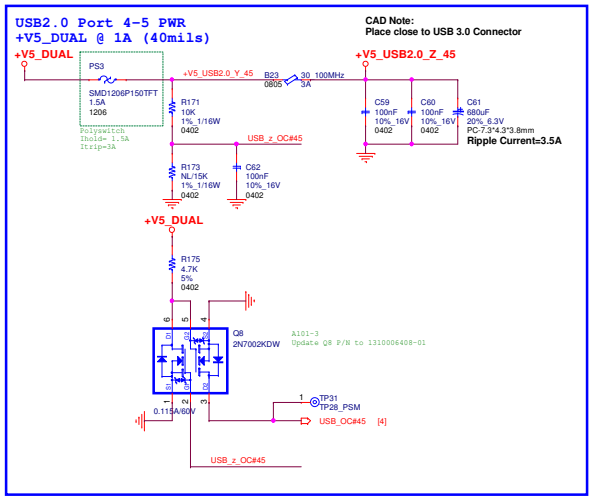
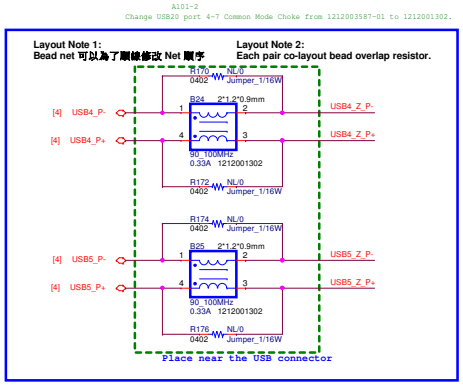
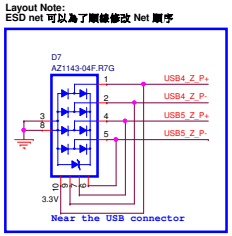
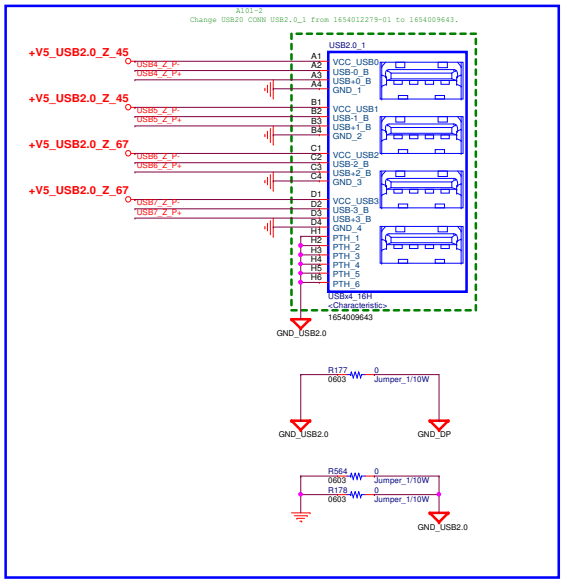
USB2.0 Port 4-5 PWR



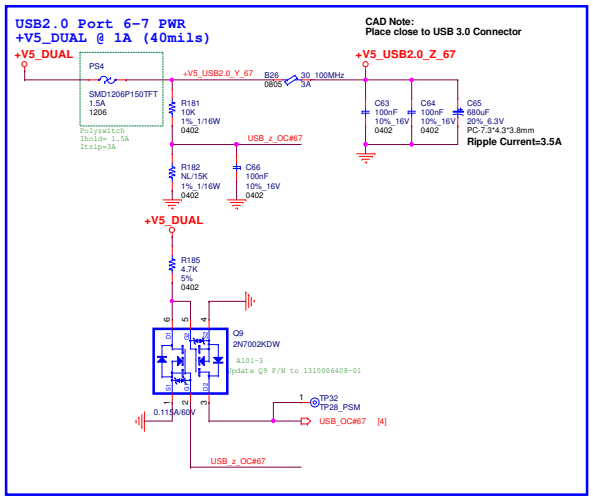


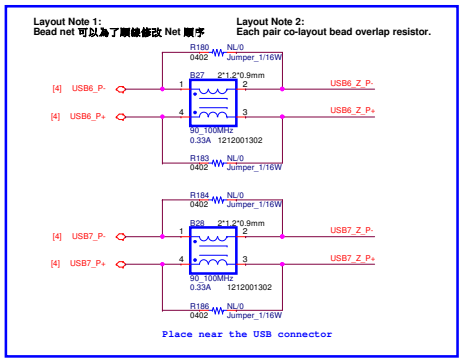


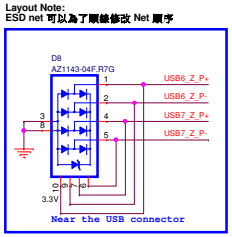
USB2.0 Port 4-7



USB2.0 Port 6-7 PWR







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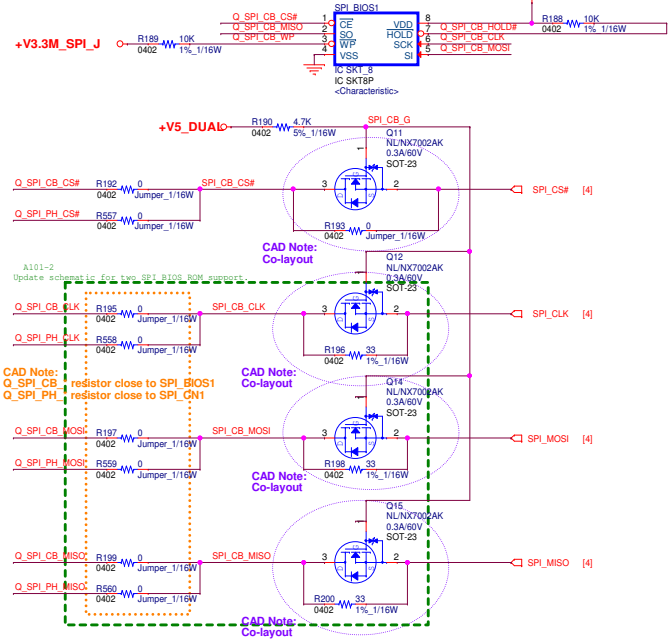
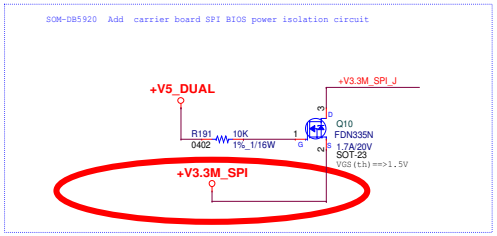
SPI

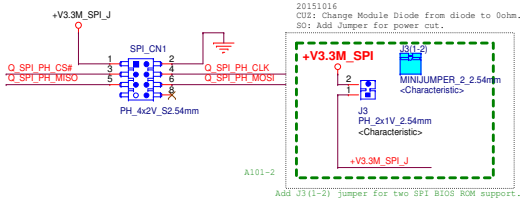
BIOS SPI

+V3.3M_SPI @ 100mA

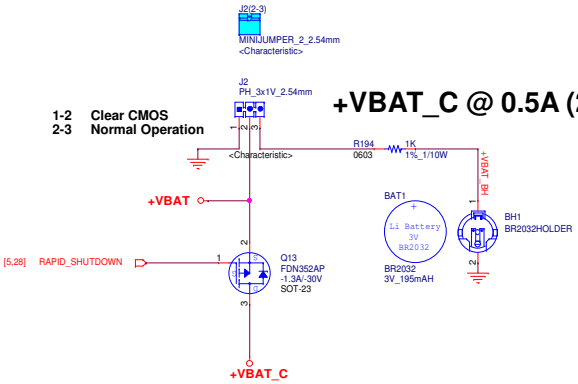
With COM.0 Rev 3, the SPI interface maybe either 3.3V or 1.8V, as is best for the Module chipset at hand.



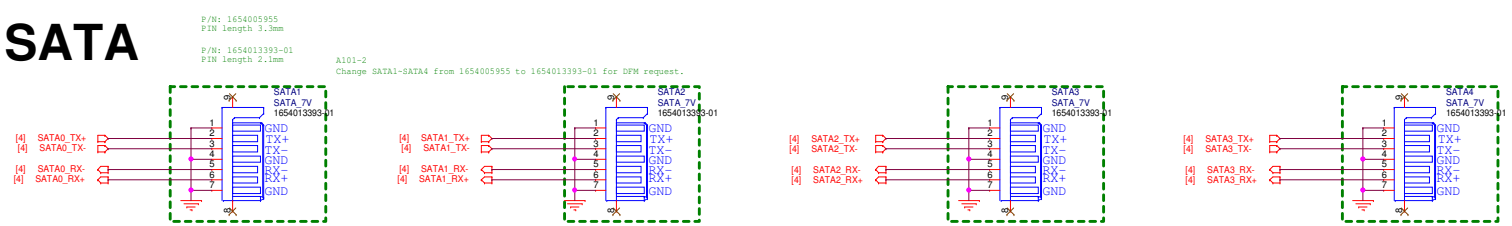




RTC BATTERY



SATA



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Title	BIOS socket/SATA/RTC	
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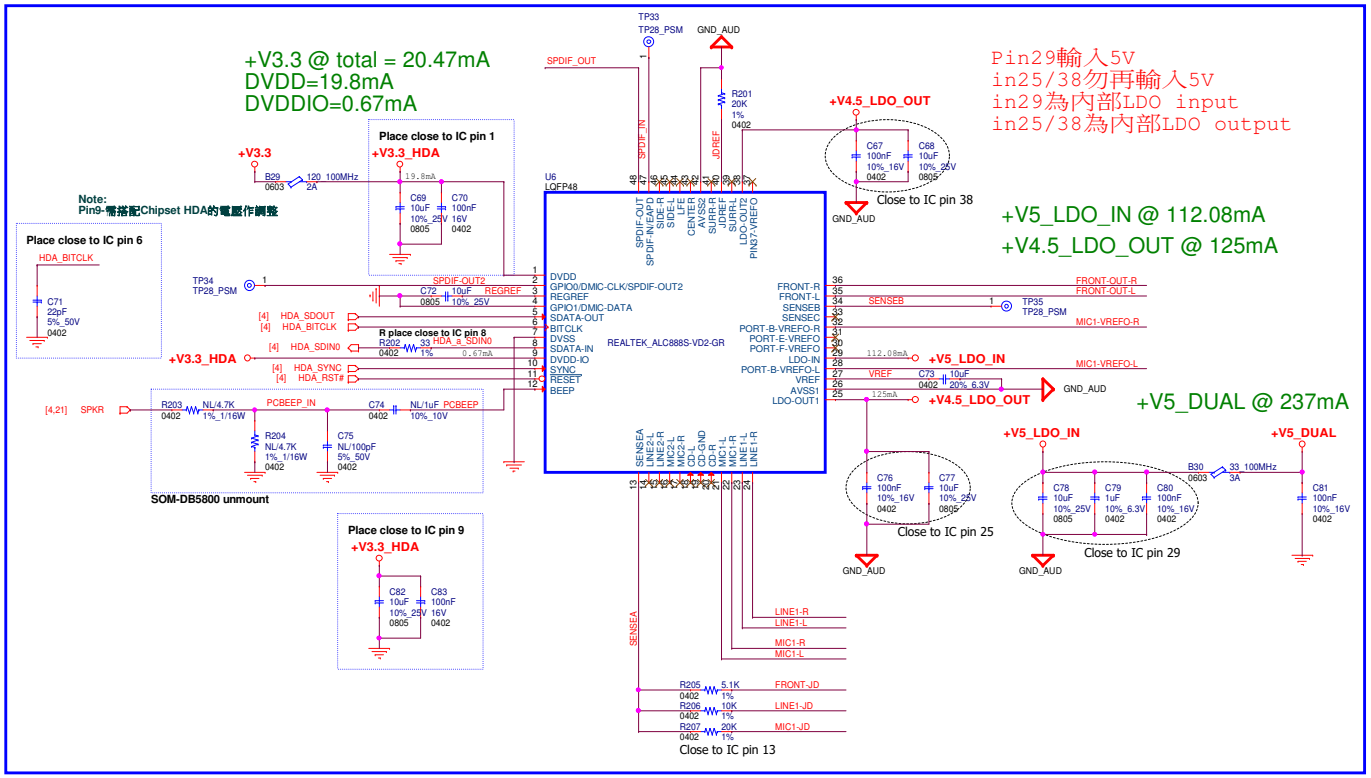
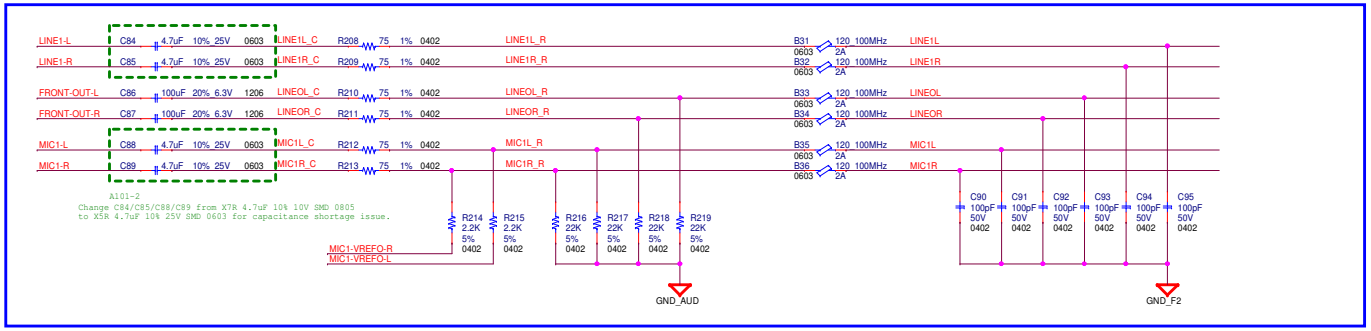
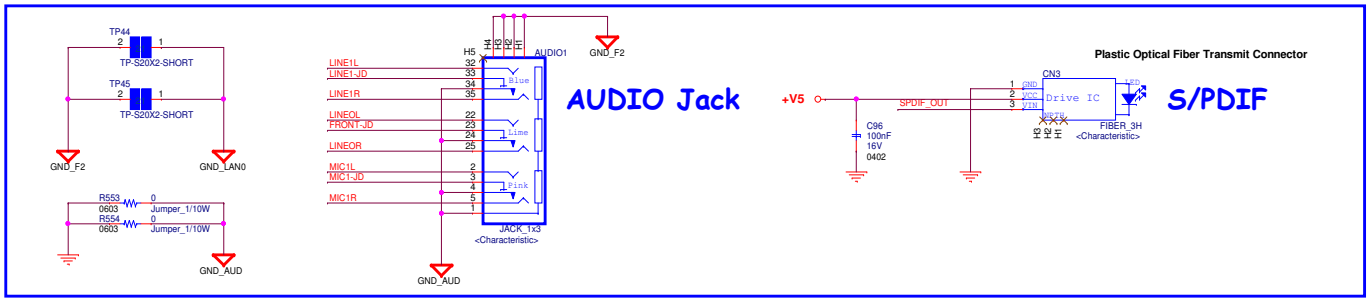
HD Audio Codec REALTEK ALC888S-VD2-GR







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Title	HD Audio Codec ALC888		
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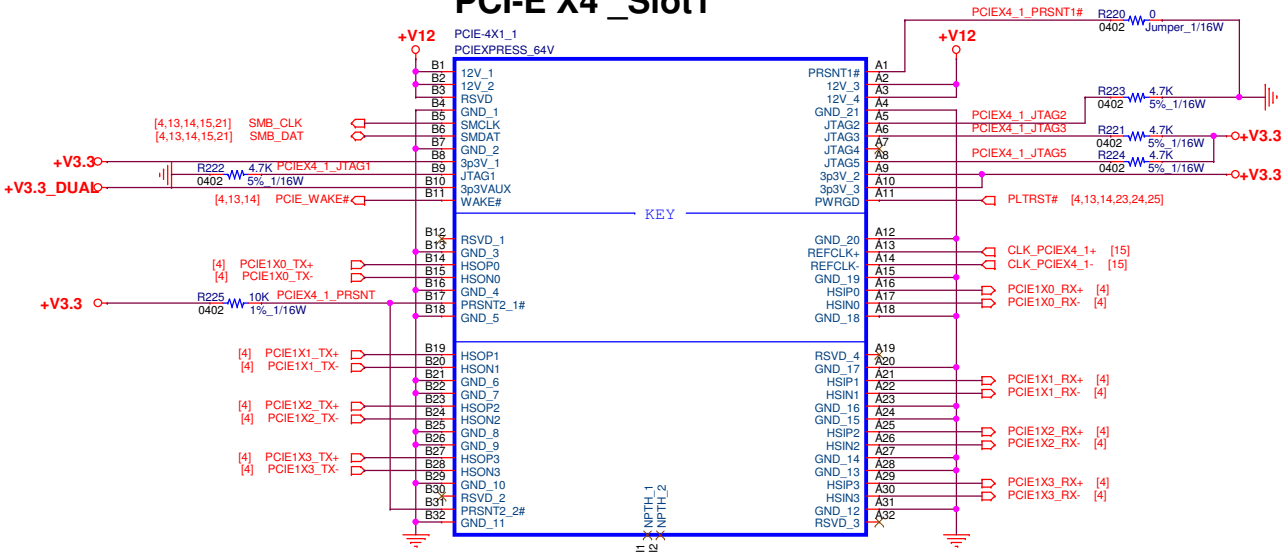
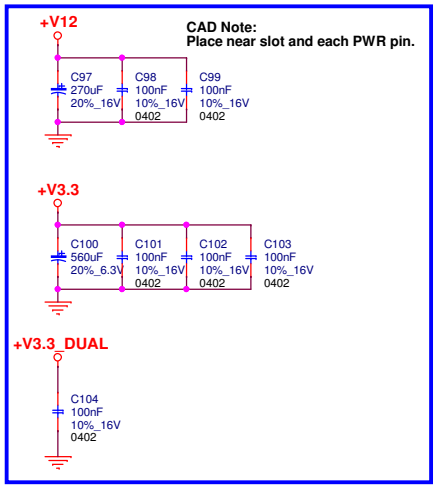
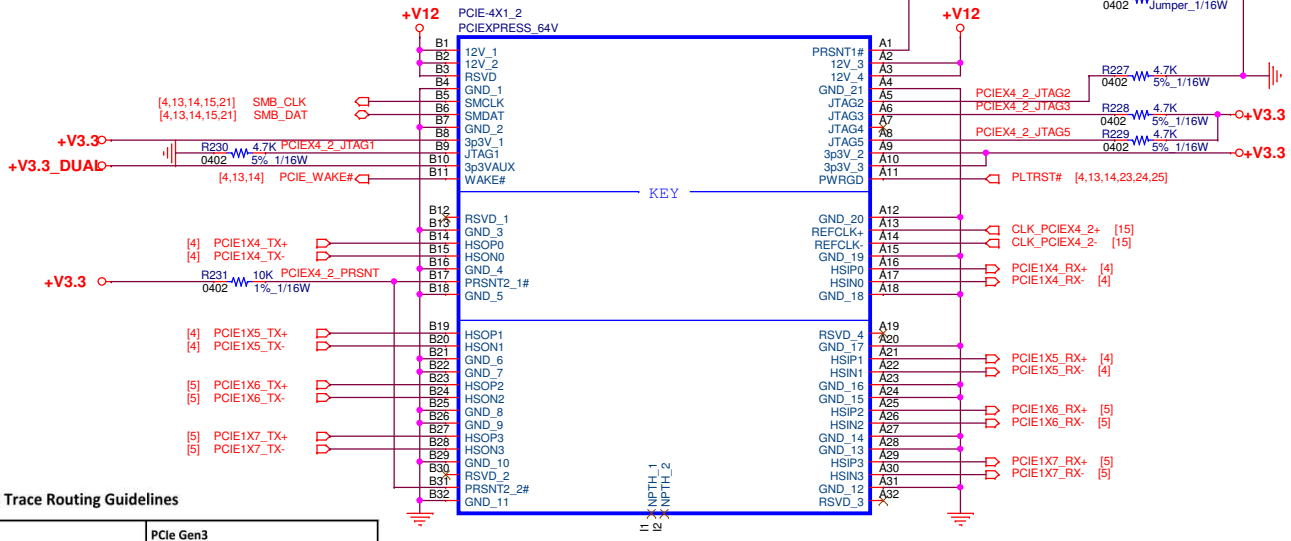
PCI-E X4 _Slot1





PCI-E X4 _Slot2



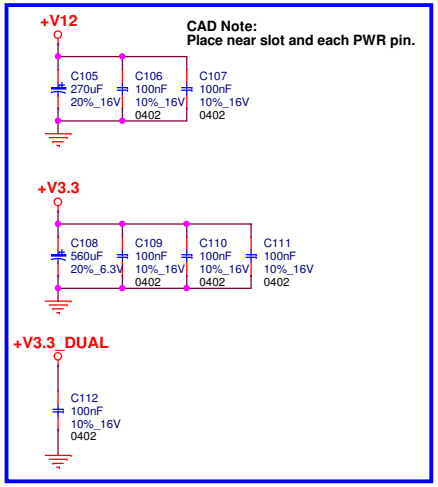


Table 5.11: PCI Express Trace Routing Guidelines

Parameter	PCIe Gen2	PCIe Gen3
Symbol Rate / PCIe Lane	5.0 G Symbols/s	8.0 G Symbols/s
Maximum signal line length (coupled traces) TX and RX	21.0 inches	14.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe device	15.85 inches	10.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe slot	9.00 inches	4.0 inches
PCI-SIG: Differential impedance recommendation	85 Ω +/-15%	85 Ω +/-15%
COMCDG Rev. 2.0: Differential impedance recommendation for new Carrier designs	85 Ω +/-15%	
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%

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Title	PCIe X4 Slot 1-2	
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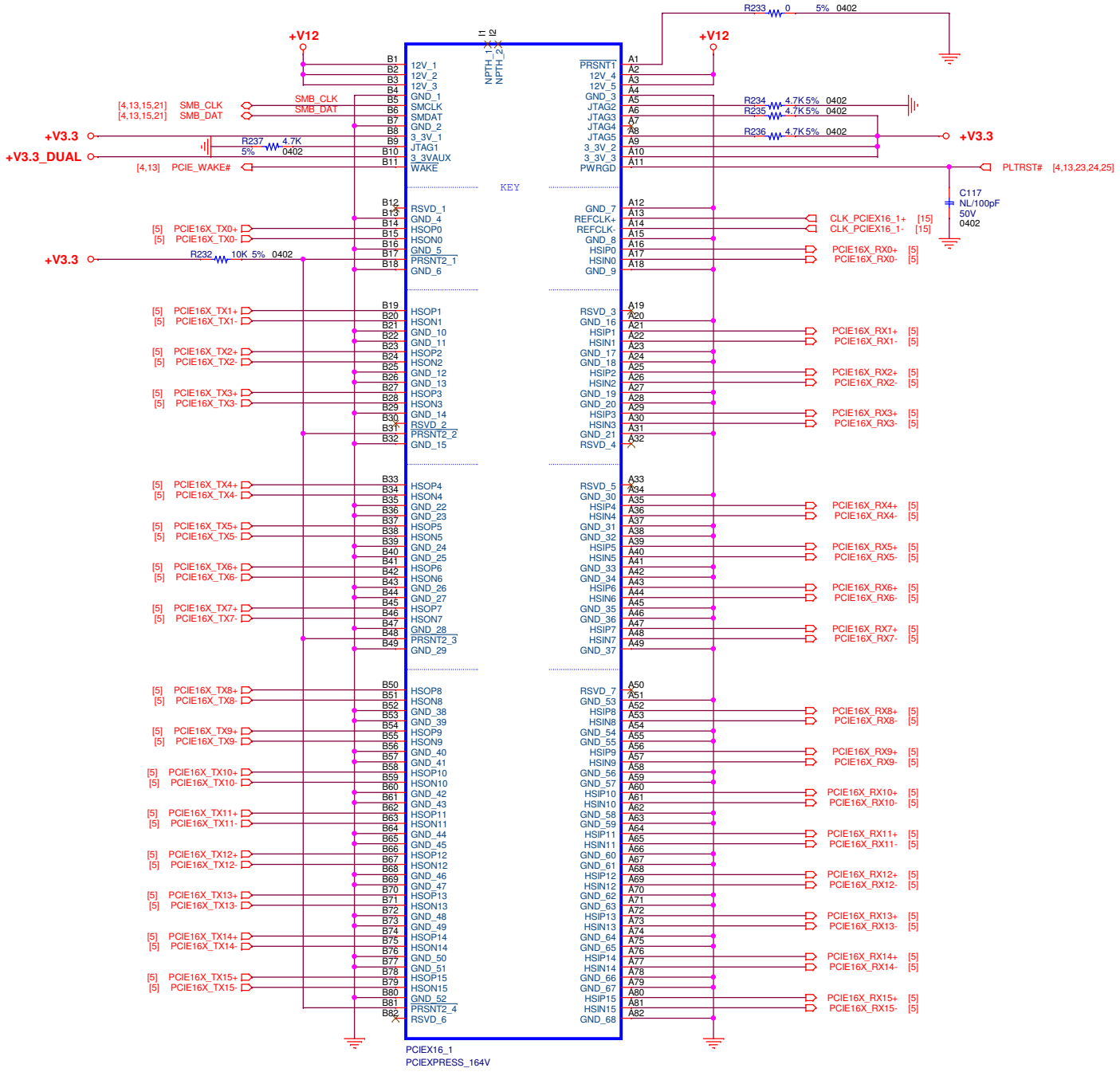
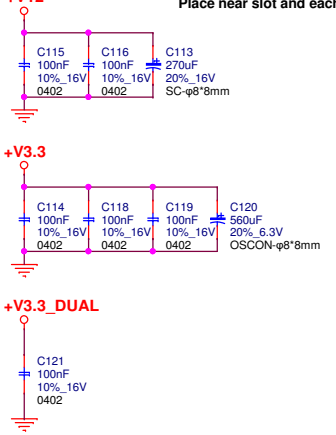


CAD Note:
Place near slot and each PWR pin.



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Title	PCI Express X16 Slot	
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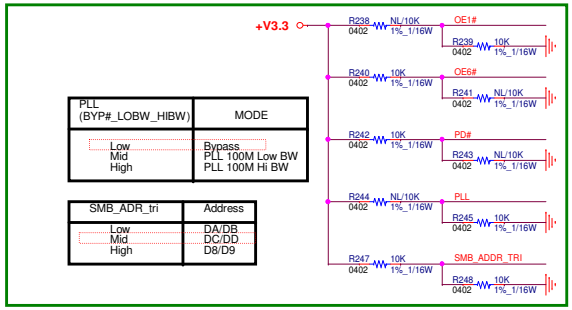
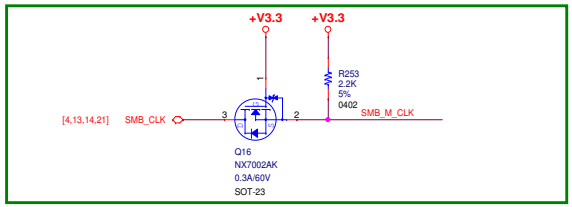
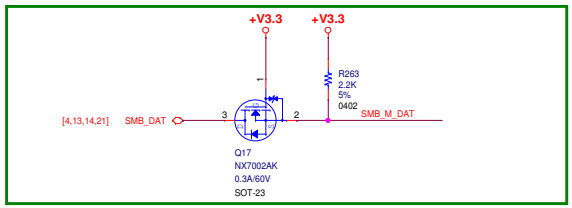
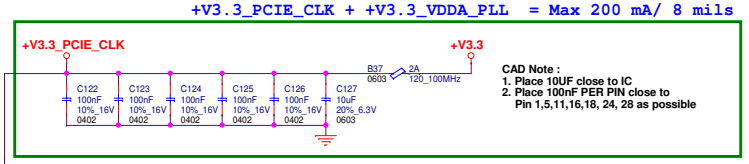
PCIE Clock Buffer

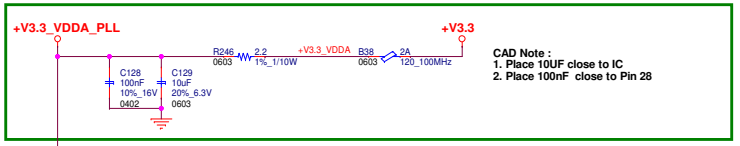




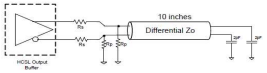


+V3.3_PCIE_CLK + +V3.3_VDDA_PLL = Max 200 mA/ 8 mils





FAE suggestion for diff. impedance 85ohm.



Differential Output Termination Table

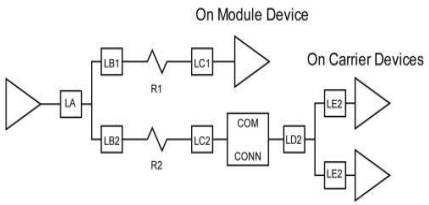
DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

5.4.9 Carrier Board LPC Devices

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads ***should*** be connected to the common clock without a buffer. The Carrier Board ***should*** not have more than two loads on the LPC clock.
Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 5-9: Typical Routing Topology for a Module LPC Device



LA 500 mils max
LB1 = LB2 = 150 mils max
LC1 = 8.88"+LC2
LC2 = .25" max
LE2 = 1" max
LD2 + LE2 (note 2 instances of LE2) = 8.88"
R1 = R2 = 22Ω

PCI Clock Buffer

+V3.3 @ Max 40 mA / 1.6 mils

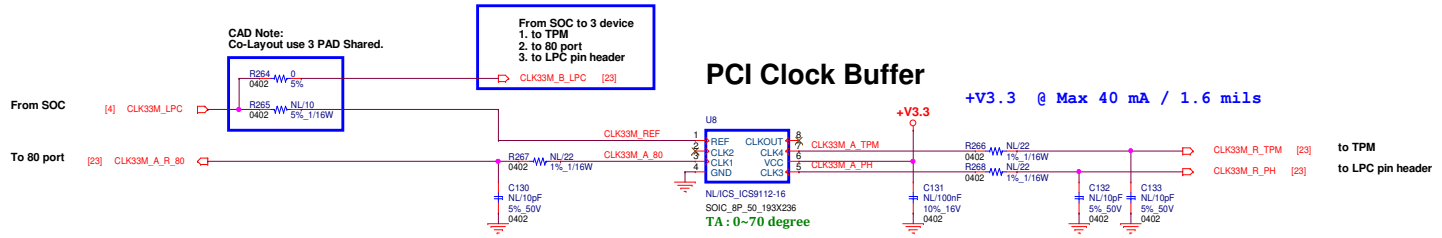


Figure 192. LPC_CLK[0] or LPC_CLK[1]Routing Topology—2 Branches Using One Clock as Output

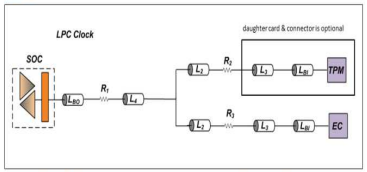


Table 132. LPC_CLK[1:0] Signals Trace Routing—2 Branches (Sheet 1 of 2)

Parameter	Trace Width (mils)	Minimum Trace Spacing (mils)	Trace Length (mils)
Breakout L_{80} and Breakin L_{81}	3.50	3.50	0–500
L1 Main Route	4mils MS 4.5mils DSL	15	500–7500
L2 Main Route	4mils MS 4.5mils DSL	15	500–2000
L3 Main Route	4mils MS 4.5mils DSL	15	500–2500

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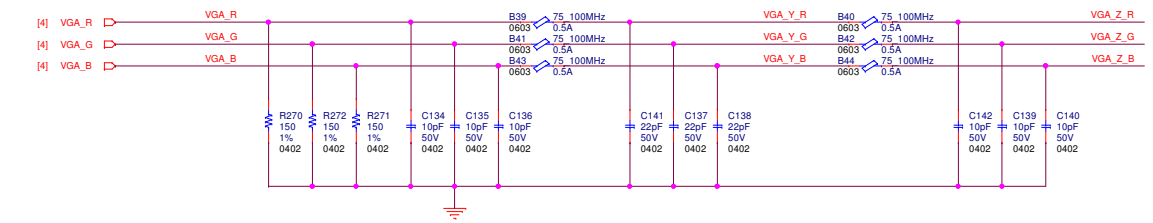
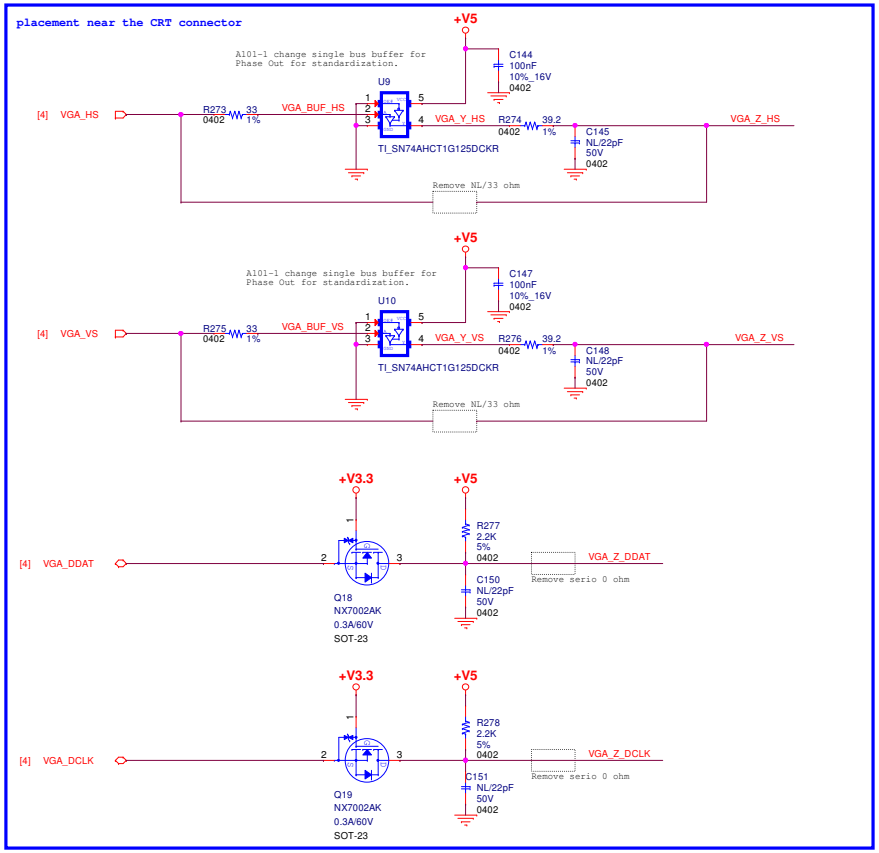
VGA

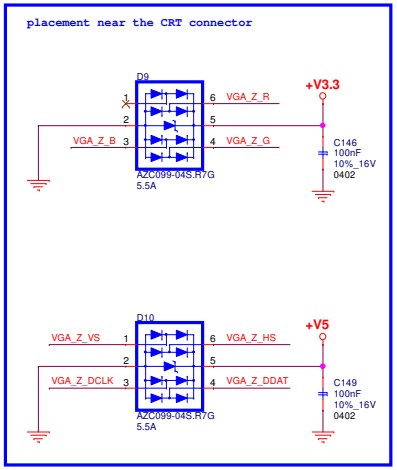
placement near the CRT connector



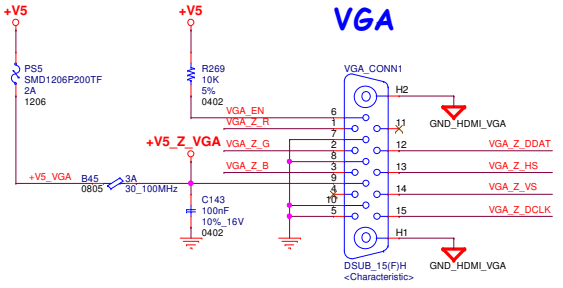
placement near the CRT connector



placement near the CRT connector



+V5 @ 1A



VGA

Oprerating Temperature: -55~105 degree

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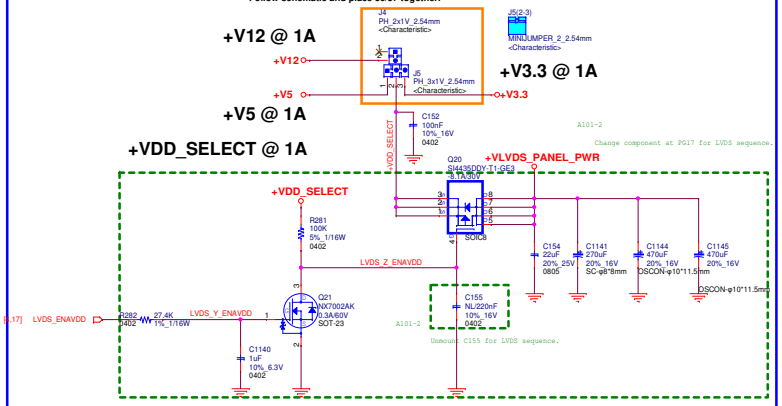
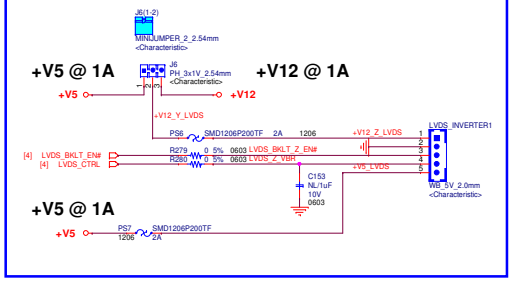
LVDS PWR selection

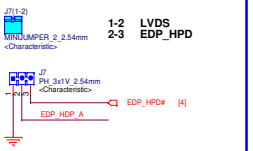
CAD Note :
Follow schematic and place J6/J7 together.



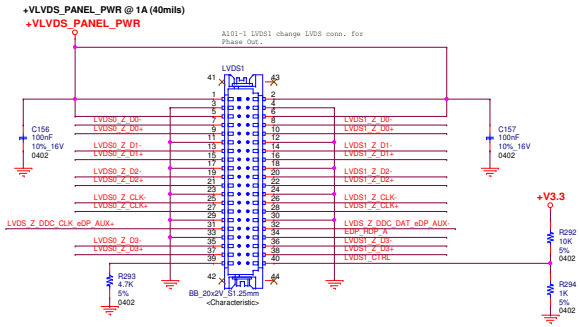
LVDS INVERTER



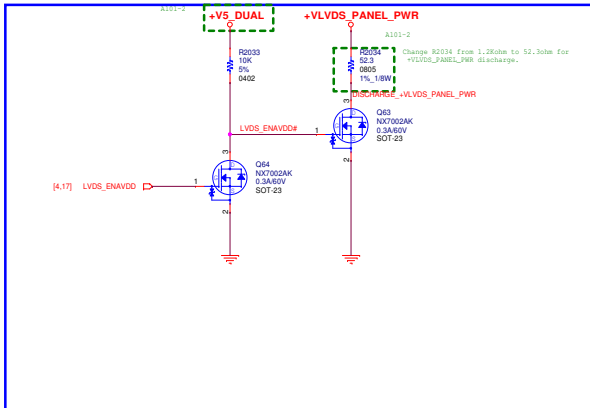
EDP / LVDS HPD selection



LVDS Connector



Discharge Circuit



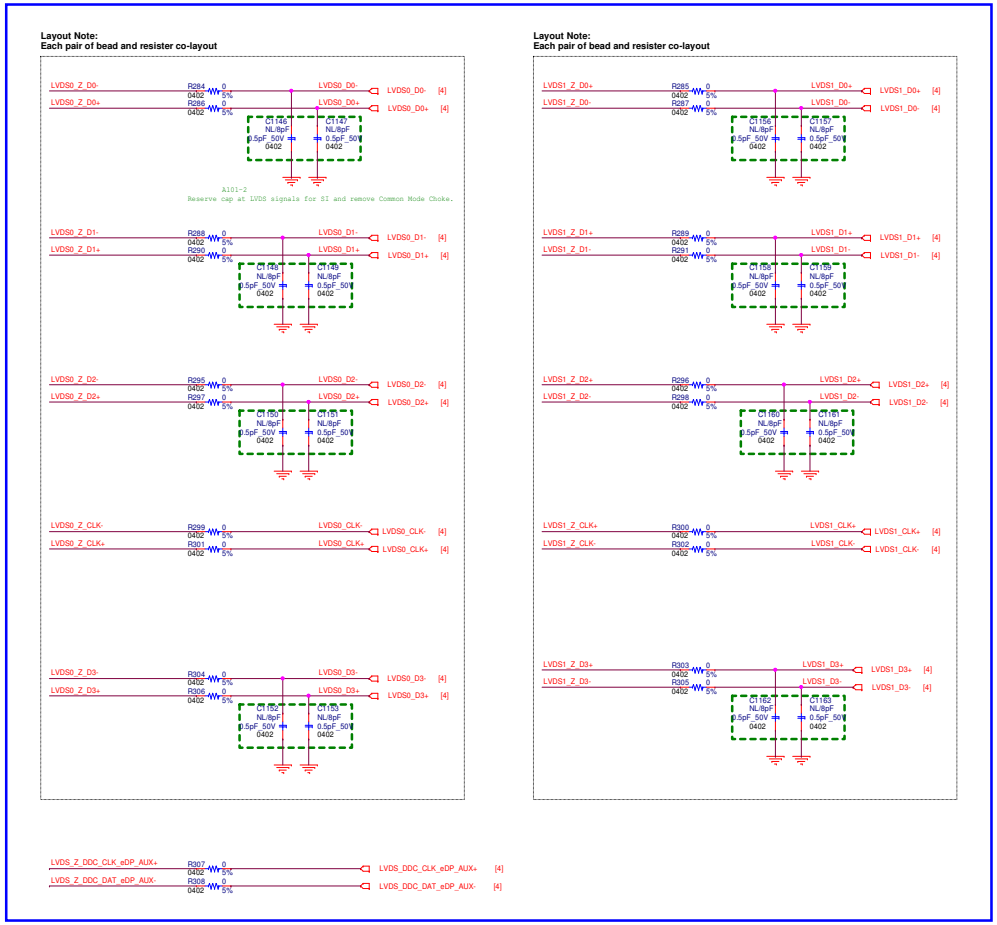


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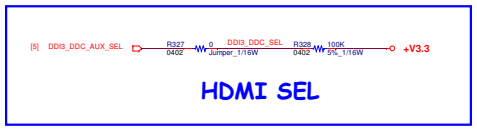
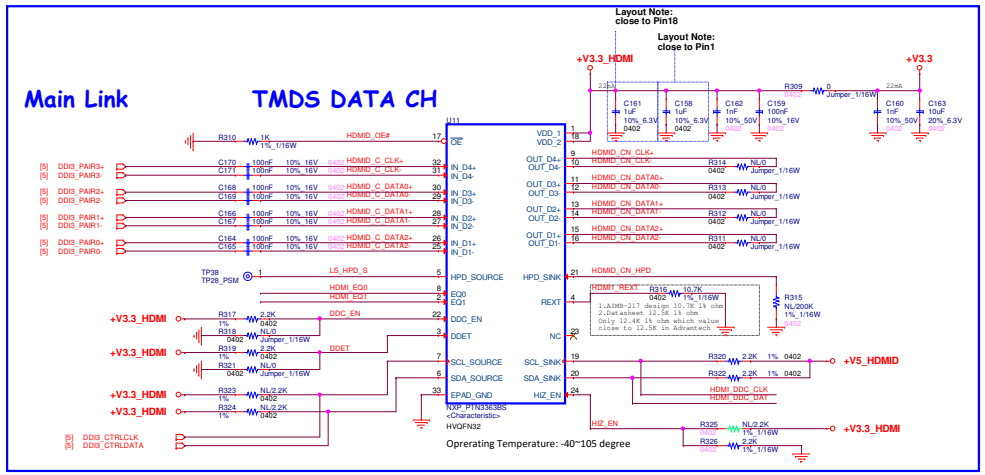
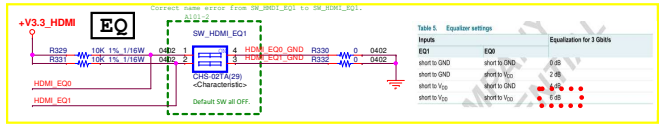
Table 11: *Display Port / HDMI / DVI Pin-out of Type 10 and Type 6*

COM Express Pin Name	DDI0 Type 10	DDI1 Type 6	DDI2 Type 6	DDI3 Type 6	Function (DDIX) DisplayPort	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	B71	D26	D39	C39	DPX_LANE0+	TMDSX_DATA2+
DDIX_PAIR0-	B72	D27	D40	C40	DPX_LANE0-	TMDSX_DATA2-
DDIX_PAIR1+	B73	D29	D42	C42	DPX_LANE1+	TMDSX_DATA1+
DDIX_PAIR1-	B74	D30	D43	C43	DPX_LANE1-	TMDSX_DATA1-
DDIX_PAIR2+	B75	D32	D46	C46	DPX_LANE2+	TMDSX_DATA0+
DDIX_PAIR2-	B76	D33	D47	C47	DPX_LANE2-	TMDSX_DATA0-
DDIX_PAIR3+	B81	D36	D49	C49	DPX_LANE3+	TMDSX_CLK+
DDIX_PAIR3-	B82	D37	D50	C50	DPX_LANE3-	TMDSX_CLK-
DDIX_HPD	B89	C24	D44	C44	DPX_HPD	HDMIX_HPD
DDIX_CTRLCLK_AUX+	B98	D15	C32	C36	DPX_AUX+	HDMIX_CTRLCLK
DDIX_CTRLDATA_AUX-	B99	D16	C33	C37	DPX_AUX-	HDMIX_CTRLDATA
DDIX_DDC_AUX_SEL	B95	D34	C34	C38		

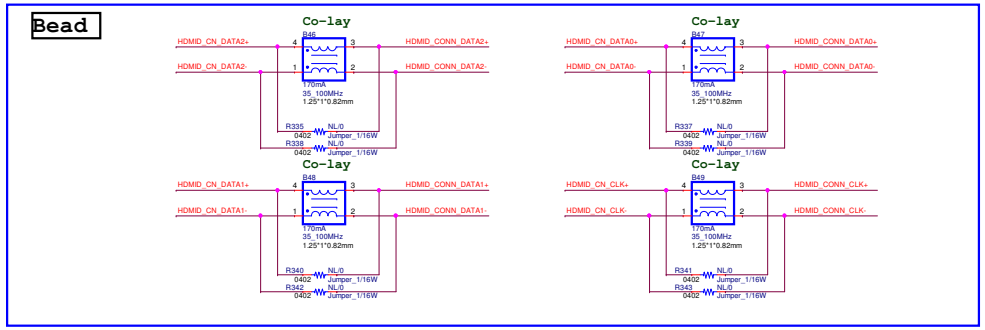


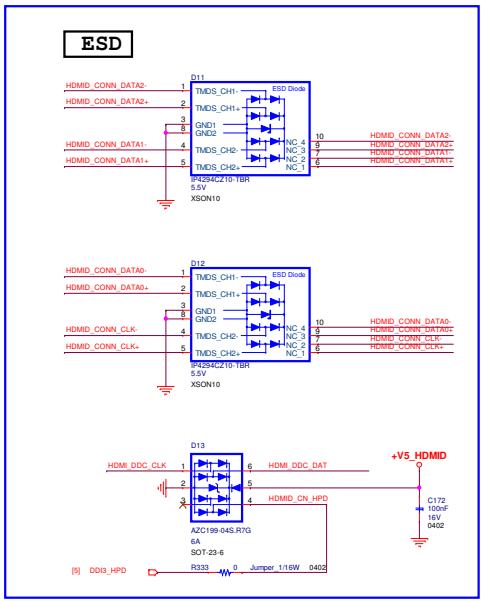


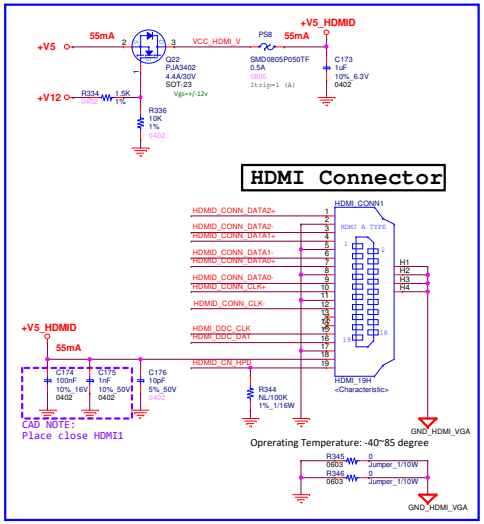


HIZ_EN=0, 50 termination resistors are enabled on IN_Dx and this configuration option is used for HDMI level shifter use case.

HIZ_EN=1, high input impedance is presented on IN_Dx and this configuration option is used when PTN3363 is used for native HDMI redriver use cases. In the native redriver use case, external 50 termination resistors on the application are pulled up to VDD.







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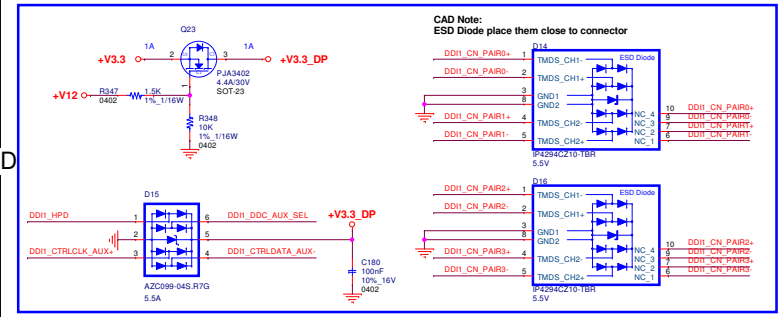
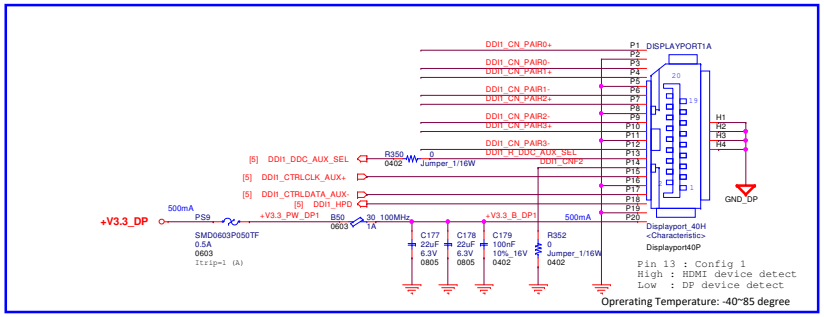
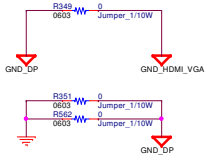
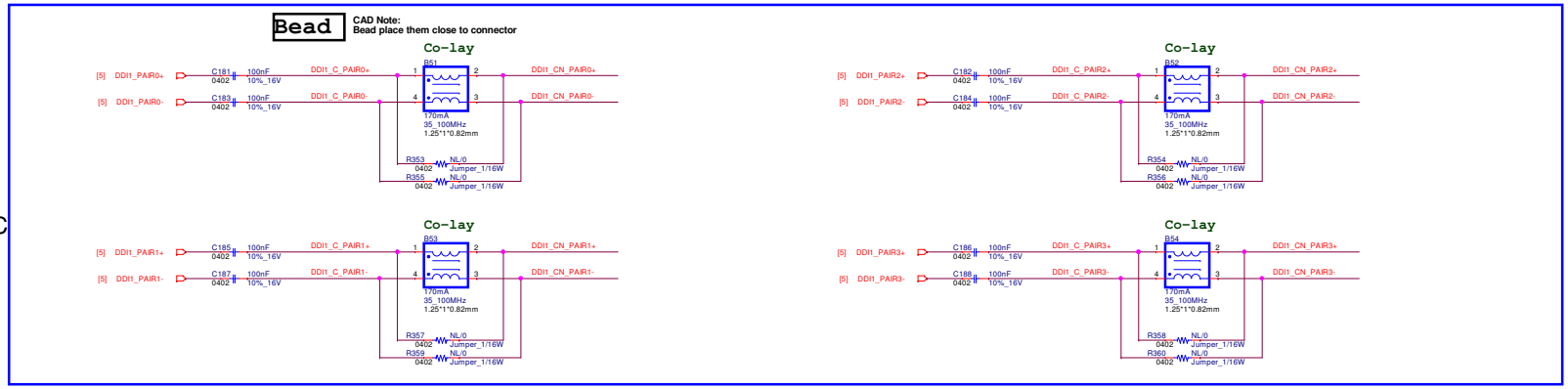
DP1

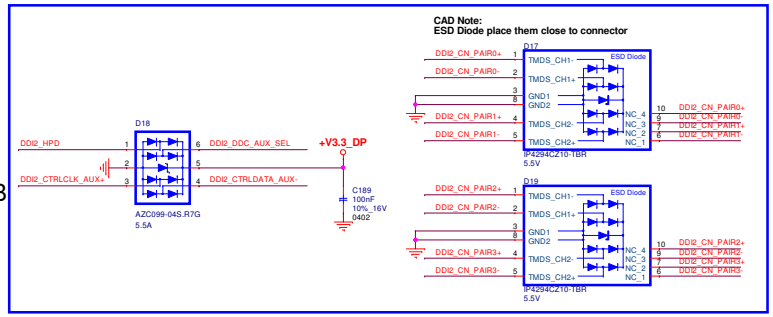


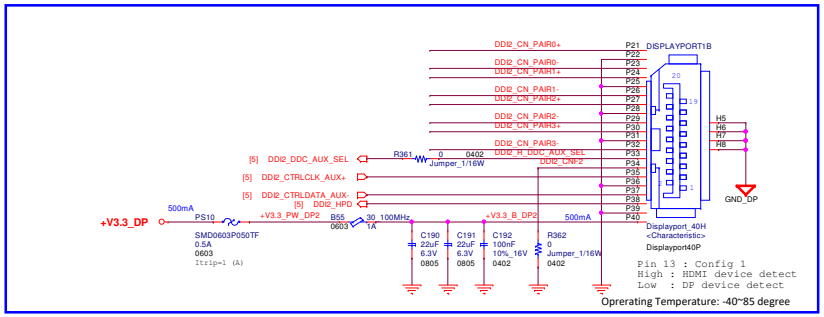


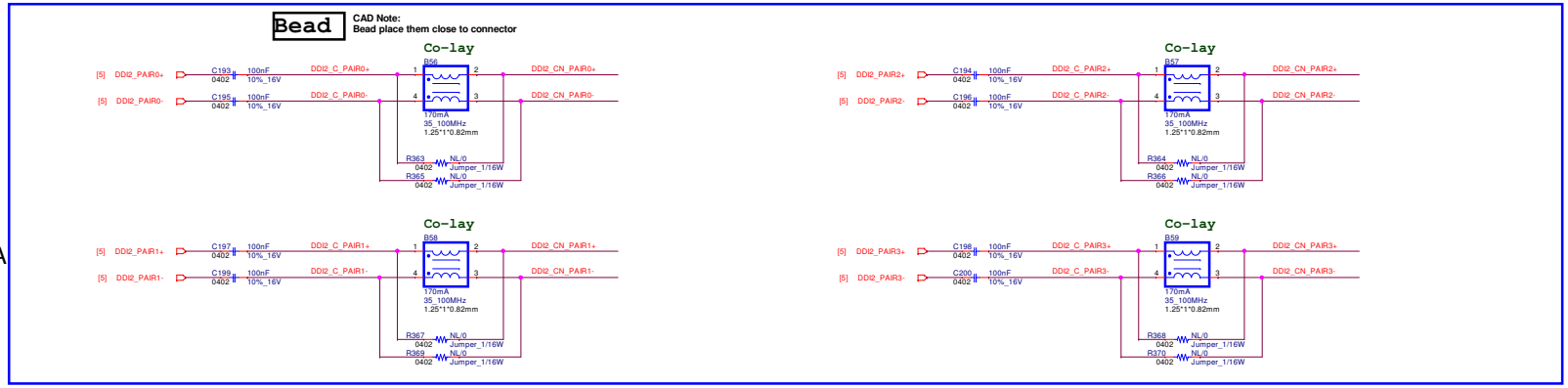




DP2







ADVANTECH

Title	DP Conn. DDI port1-2	
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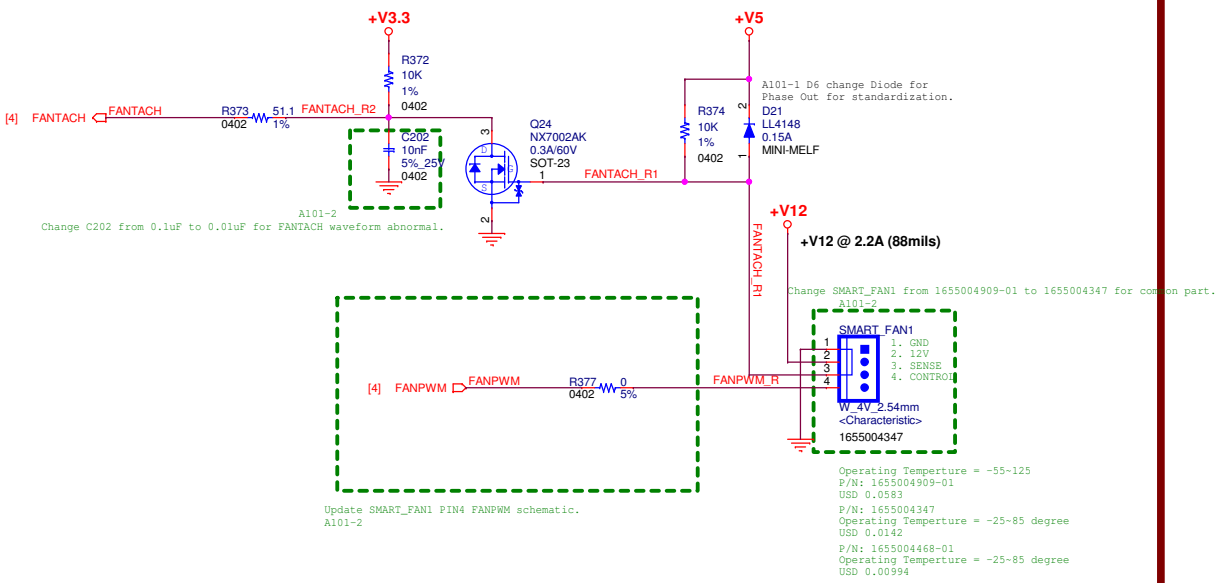
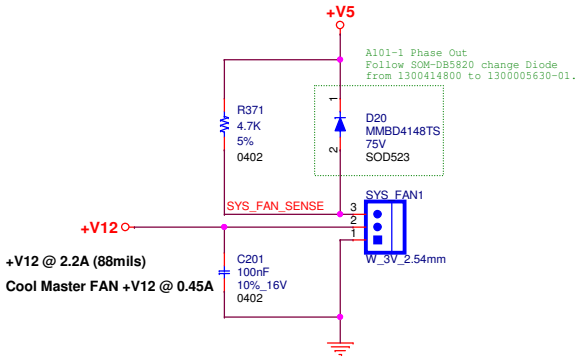
SMART FAN



SYSTEM FAN



ADVANTECH

Title	SYS FAN / SMART FAN	
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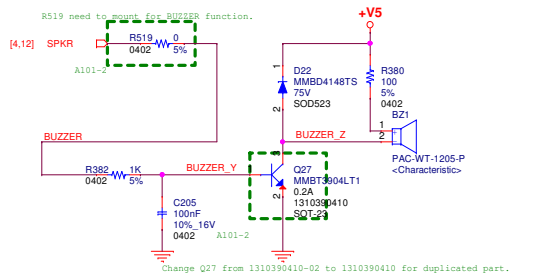
BUZZER



GPIO CONN

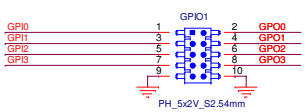
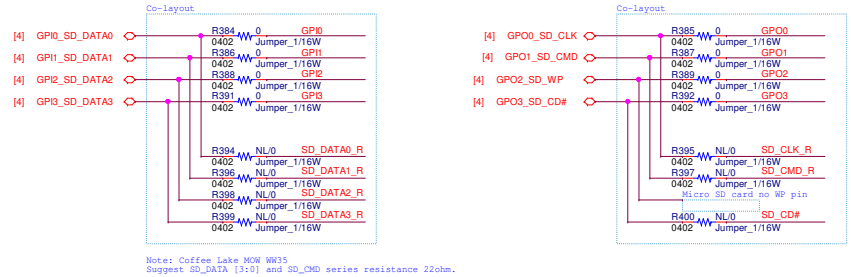


Table 4.30: SD Card Interface Signals

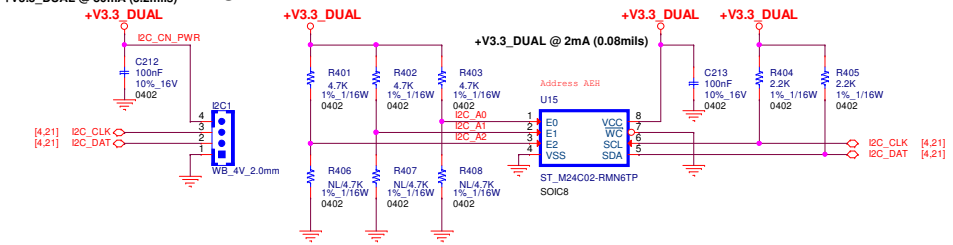
COM Express Signal	SD card interface signals	Comments
GPI0	SD_DATA0	Bidirectional signal
GPI1	SD_DATA1	Bidirectional signal
GPI2	SD_DATA2	Bidirectional signal
GPI3	SD_DATA3	Bidirectional signal
GPO0	SD_CLK	Output from COM Express, input to SD
GPO1	SD_CMD	Output from COM Express, input to SD
GPO2	SD_WP	Input to COM Express when used as SD_WP
GPO3	SD_CD#	Input to COM Express when used as SD_CD#

GPIO / SD colay

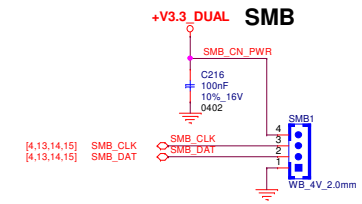


Note: Coffee Lake MOW WW35
Suggest SD_DATA [3:0] and SD_CMD series resistance 22ohm.

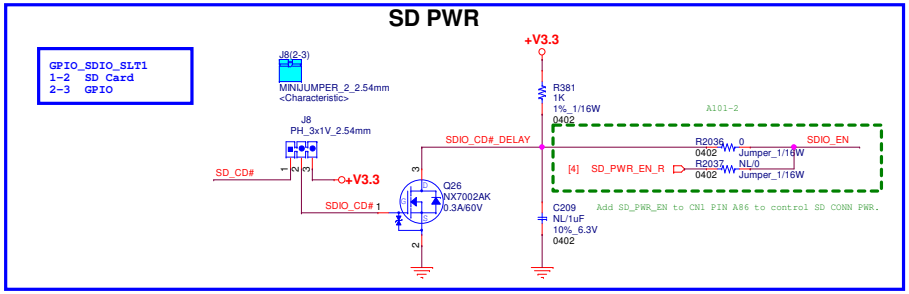
I2C



SMB

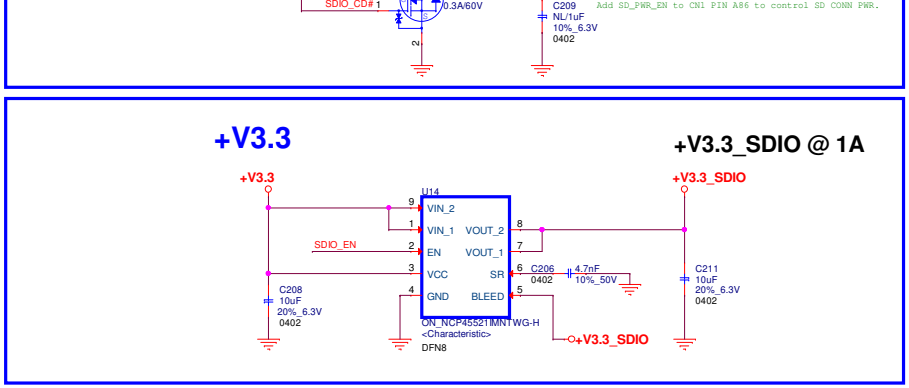


SD PWR

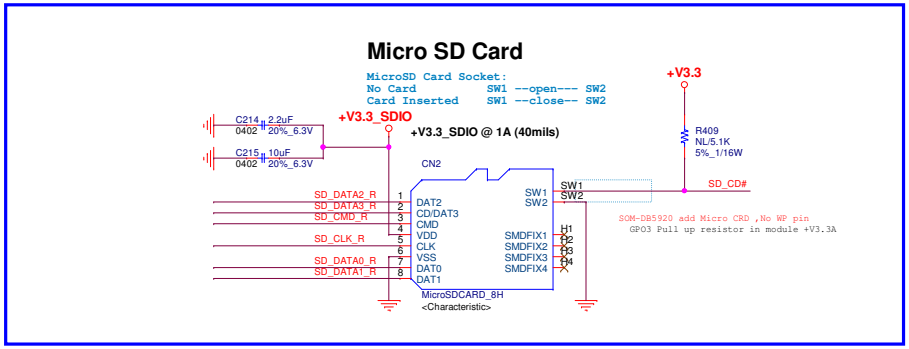


+V3.3

+V3.3_SDIO @ 1A



Micro SD Card

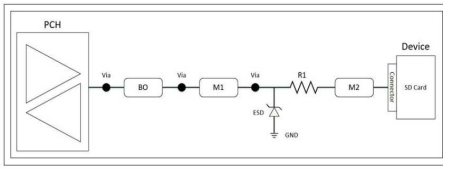


571006_CFL_MOW_WW38_2017 | 571391_CFL_H_PDG_Rev1p0

6.3.6 CFL U/S/H SDXC Guidelines Change

Description: CFL-U, S and H PCH SDXC guidelines has changed.

Resistor R1 (22 ohms) is added in the below topology diagram to be placed on SD_DATA [3:0] and SD_CMD within 12.7 mm away from the device.



Following PDGs will be updated in the next release.

ADVANTECH

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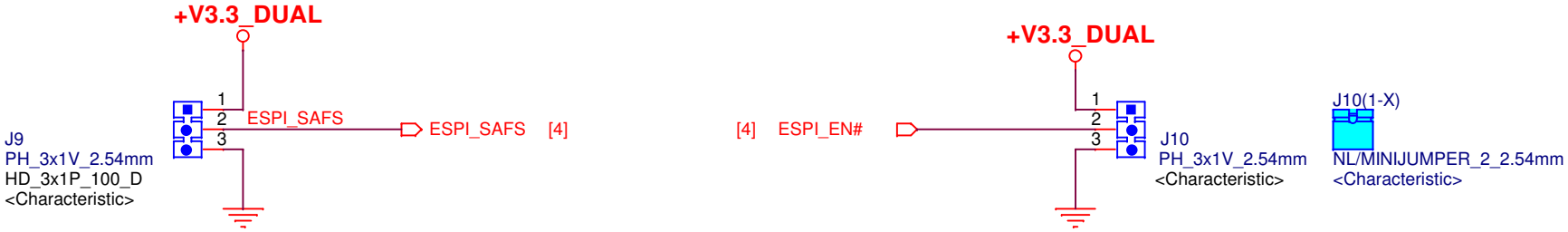
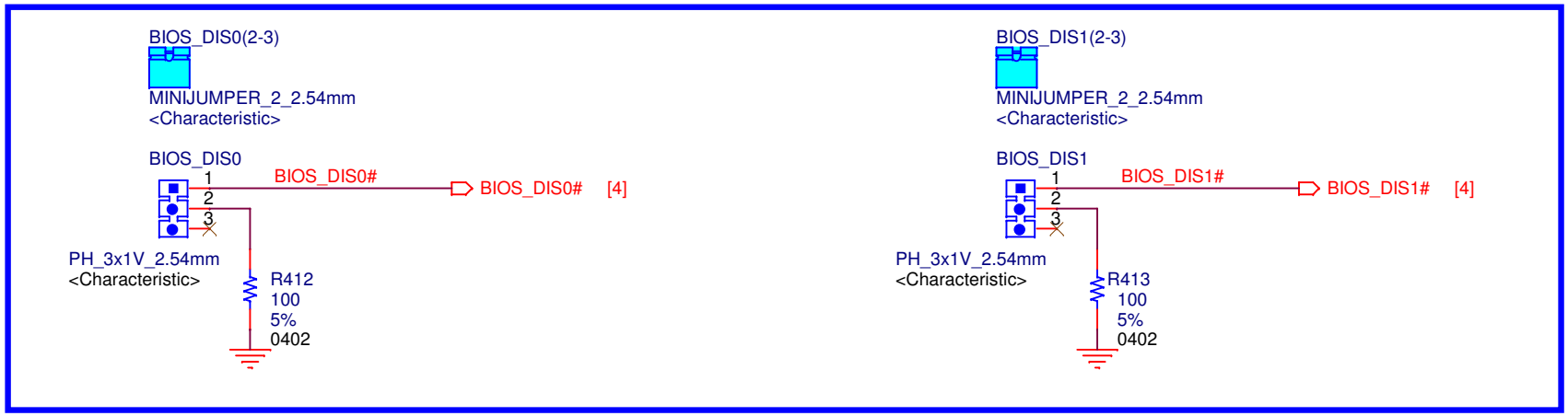
ESPI selection / BIOS selection

For COM.0 R3, the Module Carrier based BIOS options have been expanded to support eSPI devices. A third pin that affects the BIOS location, named ESPI_EN#, works in conjunction with BIOS_DIS1# and BIOS_DIS0# to define the BIOS boot path.



1.The Carrier shall leave the ESPI_EN# unconnected on the Carrier for LPC operation.
2. The Carrier shall tie ESPI_EN# to GND for eSPI operation.



ADVANTECH

Title	BIOS / eSPI selection	
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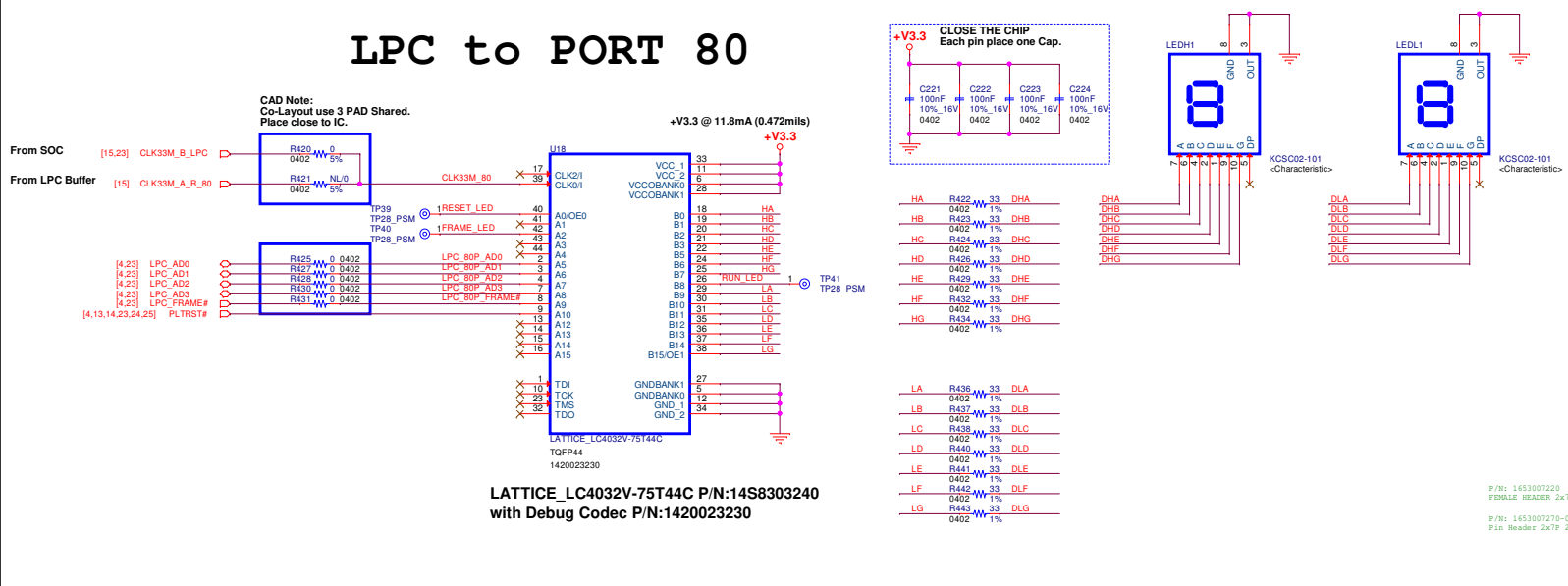
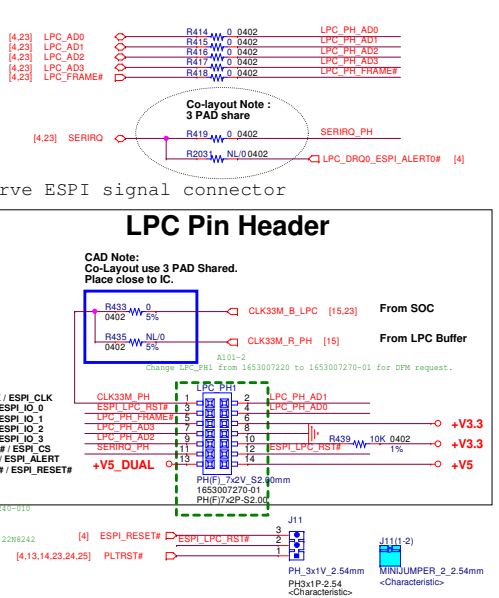
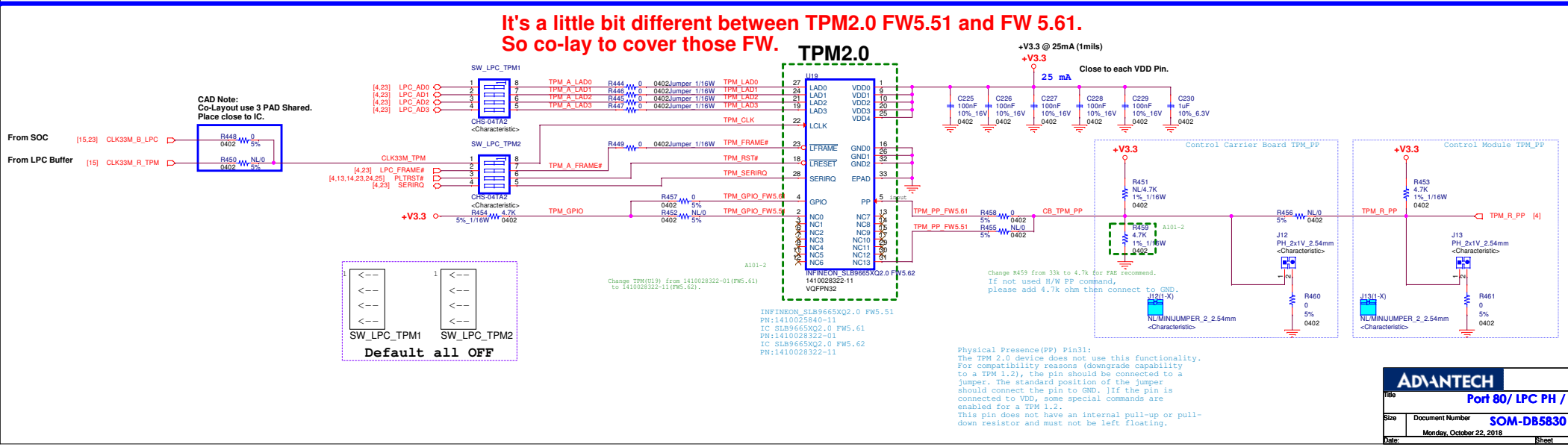
LPC to PORT 80





It's a little bit different between TPM2.0 FW5.51 and FW 5.61. So co-lay to cover those FW.



ADVANTECH			
Title	Port 80/ LPC PH / TPM		
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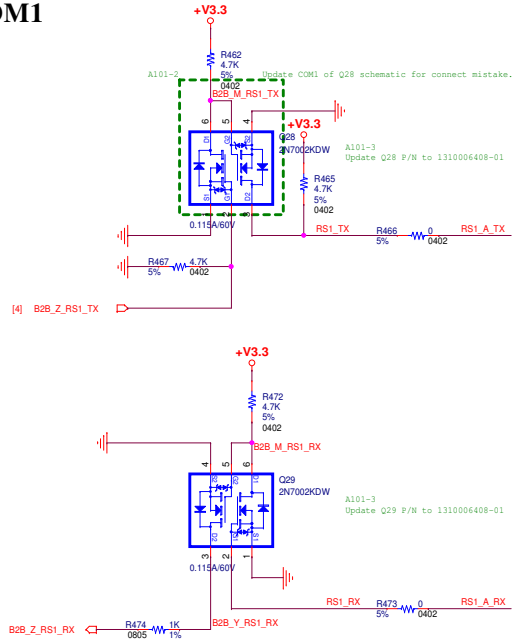
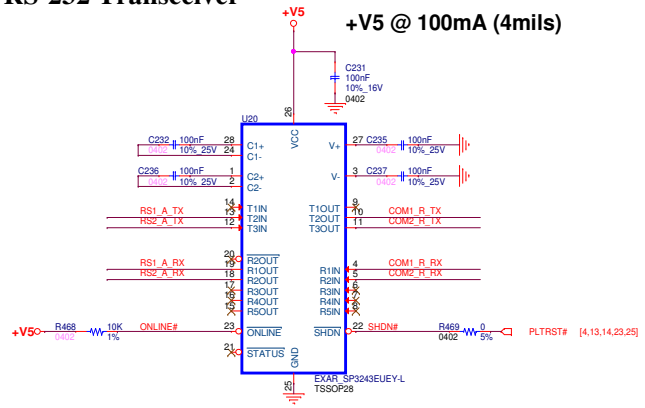
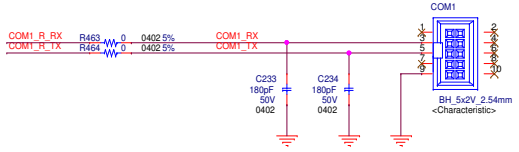
COM1



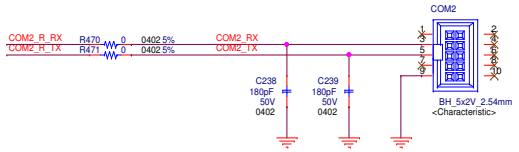
RS-232 Transceiver



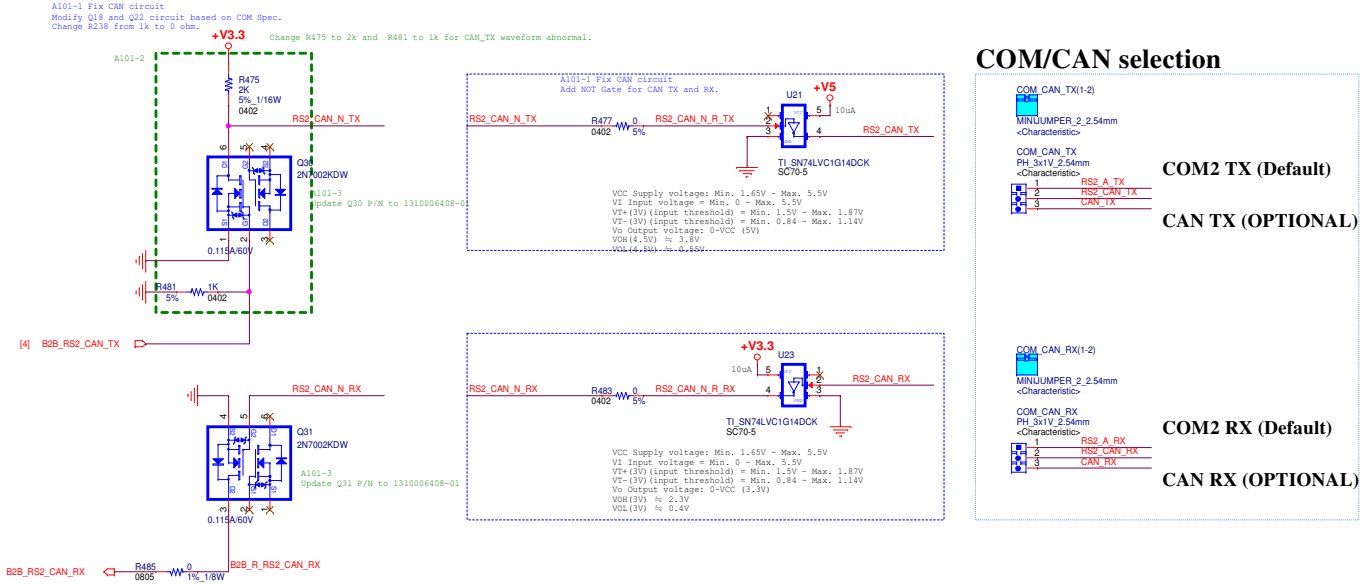
COM1 BOX HEADER



COM2 BOX HEADER

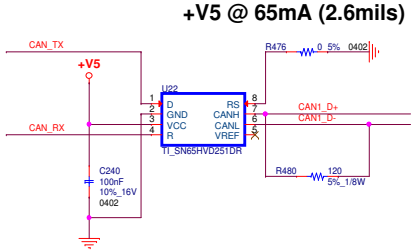


COM2 (Default) / CAN (OPTIONAL)

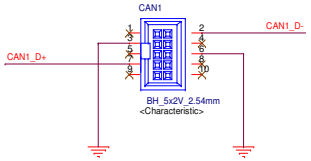


COM/CAN selection

CAN Transceiver



CAN BOX HEADER



DE-9

9 Pin (male) D-Sub CAN Bus PinOut

Pin #	Signal names	Signal Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	CAN_SHLD	Shield, Optional
6	GND	Ground, Optional
7	CAN_H	Dominant High
8	Reserved	Upgrade Path
9	CAN_V+	Power, Optional

ADVANTECH

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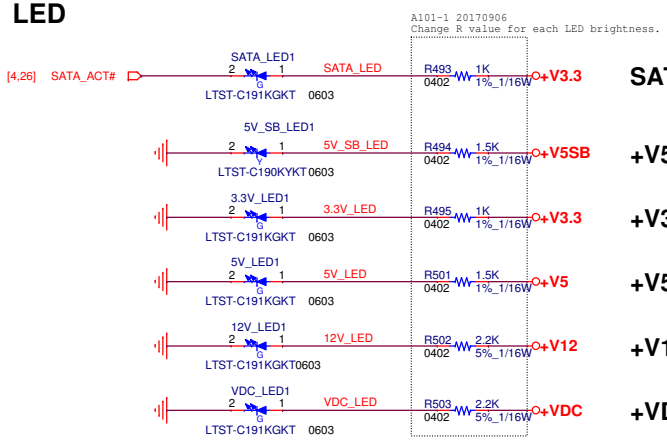
LED



SATA LED

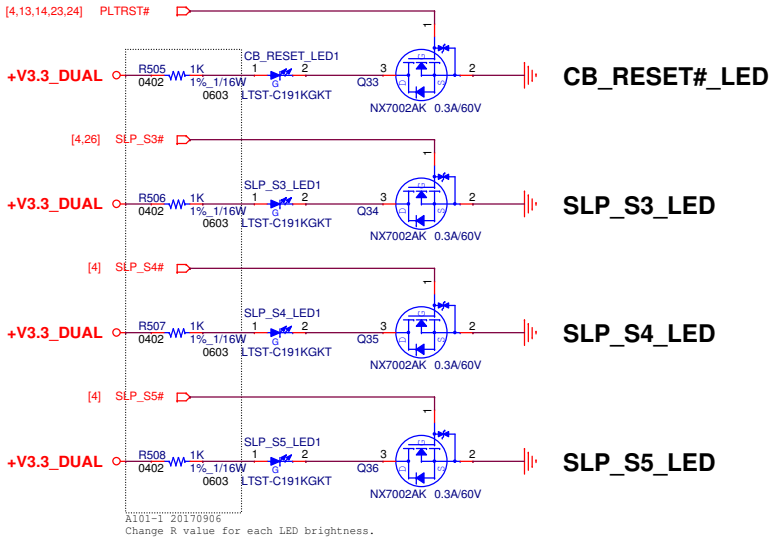
+V5SB LED

+V3.3 LED

+V5 LED

+V12 LED

+VDC LED



CB_RESET#_LED

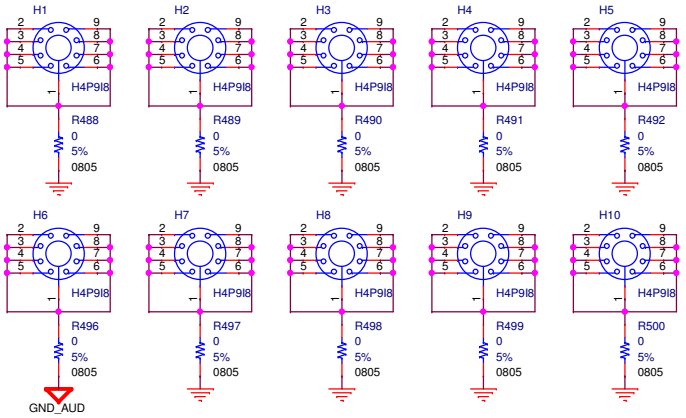
SLP_S3_LED

SLP_S4_LED

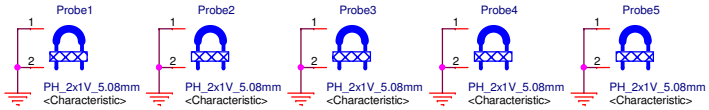
SLP_S5_LED

FM/PCB

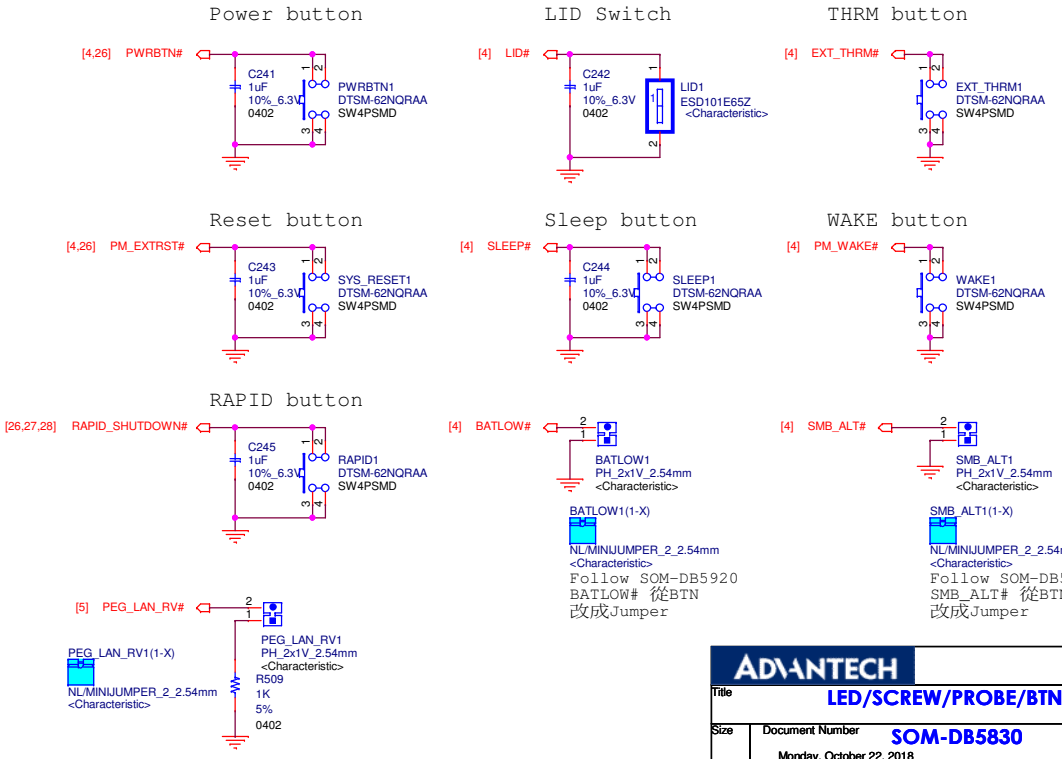
SCREW HOLE



PROBE



Button / Pin Header / Switch



ADVANTECH

Title	LED/SCREW/PROBE/BTN/PCB/FM	
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+V12 @ 24A
+V5 @ 15A
+V3.3 @ 20A
+V5SB @ 2.5A

ATX12V POWER

ATX1
ATX_12x2V_4.2mm
-V12 not used
Q37 NX7002AK 0.3A/60V SOT-23
Q38 NX7002AK 0.3A/60V
CN_PSON#
PWR_OK
R510 4.7K 0402 5%
R511 4.7K 0402 5%
RAPID_SHUTDOWN# [25,26,27,28]
PSON1 PH_3x1V_2.54mm <Characteristic>
PSON1(2-3) MINIJUMPER_2_2.54mm <Characteristic>
PSON# [27]
R513 0 0402 Jumper_1/16W
TYPE_PSON
TYPE_A_PSON
R514 NL/0 0402 Jumper_1/16W
SLP_S3# [4,25,26]
U24 TI_SN74LVC1G08DCK SC70-5
TYPE2
SLP_S3# [4,25,26]
+V3.3_DUAL
R512 4.7K 5% 0402
J14(1-2) MINIJUMPER_2_2.54mm <Characteristic>
J14 PH_2x1V_2.54mm <Characteristic>
TYPE2_A
Q39 NX7002AK 0.3A/60V SOT-23
R515 4.7K 5% 0402
Q161 NX7002AK 0.3A/60V SOT-23
U121 TI_SN74AHC1G86 SOT-23-5
R2038 4.7K 5% 0402
R2739 4.7K 5% 0402
TYPE2# [5]
TYPE0# [5]
A101-2

PSON1 Power Setting
1-2 AT Mode
2-3 ATX Mode

XOR Gate Table

Pin1	Pin2	Out
0	0	0
0	1	1
1	0	1
1	1	0

Add schematic for TYPE2# & TYPE0# select.

Type2#	Type1#	Type0#	COMe R3.0 support Type	SOM-DB5830 remark
X	X	X	Pin-out Type10	Support
NC	NC	NC	Pin-out Type2	Does not support
GND	NC	NC	Pin-out Type6	Support
GND	NC	GND	Pin-out Type7	Does not support

Layout note: Placement close ATX1

C246 270uF 20%_16V
C247 100nF 10%_16V 0402
C248 560uF 20%_6.3V
C249 100nF 10%_16V 0402
C250 560uF 20%_6.3V
C251 100nF 10%_16V 0402
C252 560uF 20%_6.3V
C253 100nF 10%_16V 0402

+V5@16A

24D14 VIA *16

+V5_DUAL@16A

24D14 VIA *16

Q40 PE632BA 53A/-30V PDFN8
Q41 PE537BA -33A/-30V PDFN8
R516 4.7K 5%_1/16W 0402
R517 4.7K 5%_1/16W 0402
5VDUAL_GATE
C254 560uF 20%_6.3V
C255 100nF 10%_16V 0402
C256 100nF 10%_16V 0402
Q42 NX7002AK 0.3A/60V SOT-23
Q43 NX7002AK 0.3A/60V SOT-23
U25 TI_SN74LVC1G17DCKR SC70-5 <Characteristic>
C257 100nF 0402 10%_16V
R520 100K 1%_1/16W 0402
PWR_OK
[4,27] CB_PWROK
+V5SB_CB
Follow SOM-DB5920 +V5_SB add Soft Start circuit to fix +V5SB inrush current issue.
R523 1210 NL/0 Jumper_1/2W
A101-1 Phase Out for standardization Change from 1310003915 to 1310005815-01.

+V5SB from PWR Supply

+V5SB @ 2.5A
VIA24D14 Via X 3

Q44 PE537BA -33A/-30V PDFN8
Rds(on)Max=8.5m Ohm @ -10V
Rds(on)Max=14m Ohm @ -4.5V
C258 4.7uF 10%_25V 0603
R524 1M 1%_1/16W 0402
V5SB_GATE#
R525 4.7K 0402 5%
R526 20K 1%_1/16W 0402
Q45 NX7002AK 0.3A/60V SOT-23
[25,26,27,28] RAPID_SHUTDOWN#

+V5SB_CB @ 2.5A
VIA24D14 Via X 3

A101-1 20170906
Reserve those pin header after RD internal meeting.

PWRBTN Pin Header

[4,25] PWRBTN#
PWRBTN_PH1 PH_2x1V_2.54mm <Characteristic>
PWRBTN_PH1(1-X) NL/MINIJUMPER_2_2.54mm <Characteristic>

SYS RESET Pin Header

[4,25] PM_EXTRST#
SYS_RESET_PH1 PH_2x1V_2.54mm <Characteristic>
SYS_RESET_PH1(1-X) NL/MINIJUMPER_2_2.54mm <Characteristic>

SATA ACT# Pin Header

R522 330 5% 0402
HDD_LED
[4,25] SATA_ACT#
SATA_ACT_PH1 PH_2x1V_2.54mm <Characteristic>
SATA_ACT_PH1(1-X) NL/MINIJUMPER_2_2.54mm <Characteristic>

Power LED Pin Header

R518 330 5% 0402
PWR_LED
PWR_LED_PH1 PH_2x1V_2.54mm <Characteristic>
PWR_LED_PH1(1-X) NL/MINIJUMPER_2_2.54mm <Characteristic>

文字面標註正極

ADVANTECH

Title	ATX power / +V5_DUAL		
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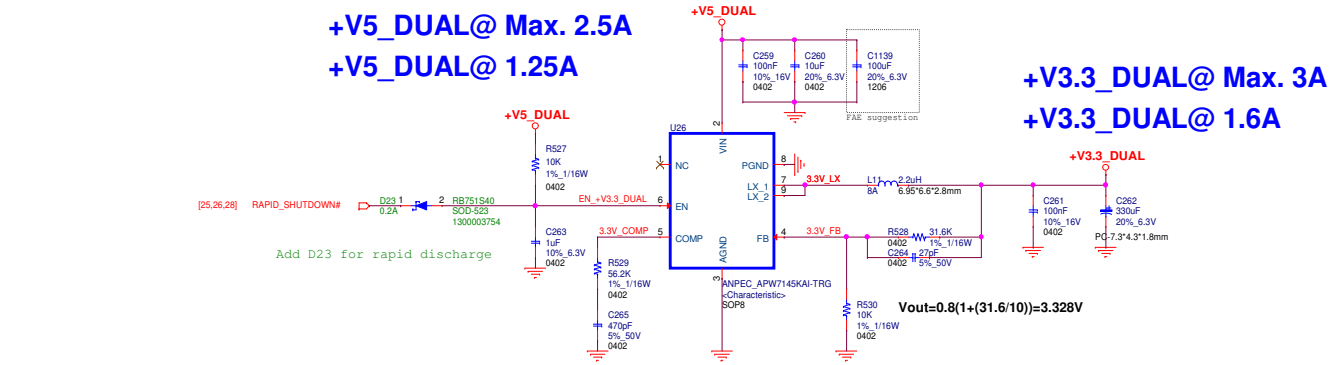
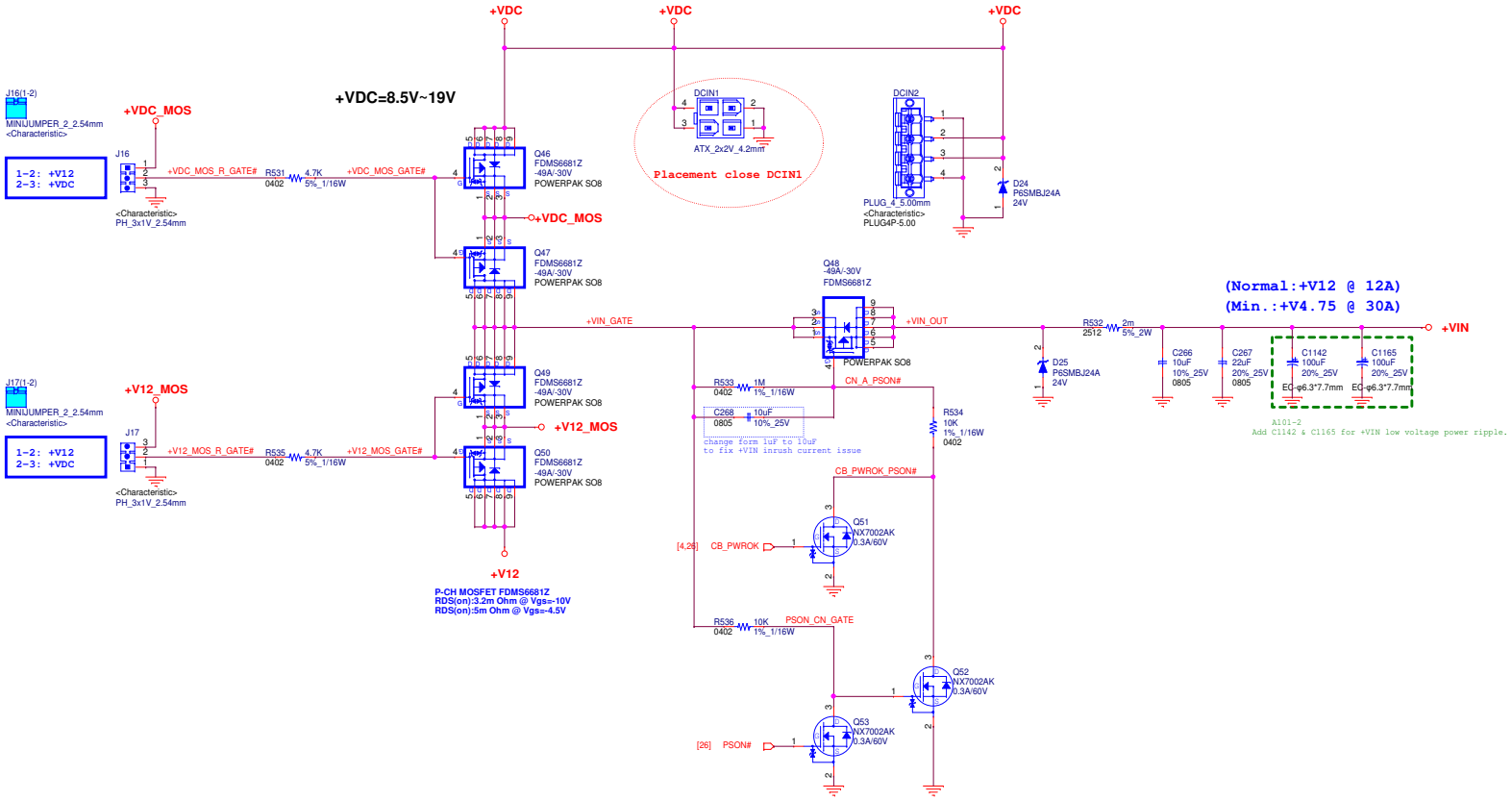
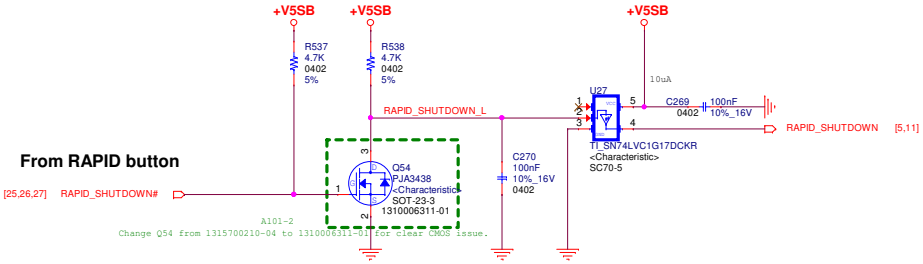

+V5_DUAL@ Max. 2.5A
+V5_DUAL@ 1.25A
+V3.3_DUAL@ Max. 3A
+V3.3_DUAL@ 1.6A
+V5_DUAL
+V3.3_DUAL
U26
ANPEC_APW7145KAI-TRG
<Characteristic>
SOP8
Add D23 for rapid discharge
Vout=0.8(1+(31.6/10))=3.328V

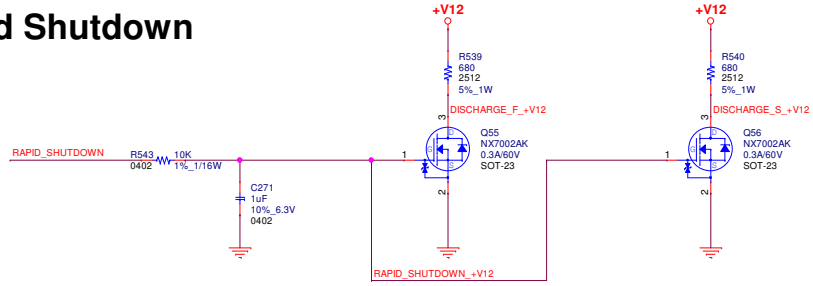

+VDC
+VDC=8.5V~19V
+VDC_MOS
+V12_MOS
+V12
Placement close DCIN1
(Normal:+V12 @ 12A)
(Min.:+V4.75 @ 30A)
+VIN
+VIN_GATE
+VIN_OUT
P-CH MOSFET FDMS6681Z
RDS(on):3.2m Ohm @ Vgs=-10V
RDS(on):5m Ohm @ Vgs=-4.5V
change form 1uF to 10uF
to fix +VIN inrush current issue
Add C1142 & C1165 for +VIN low voltage power ripple.

Rapid Shutdown



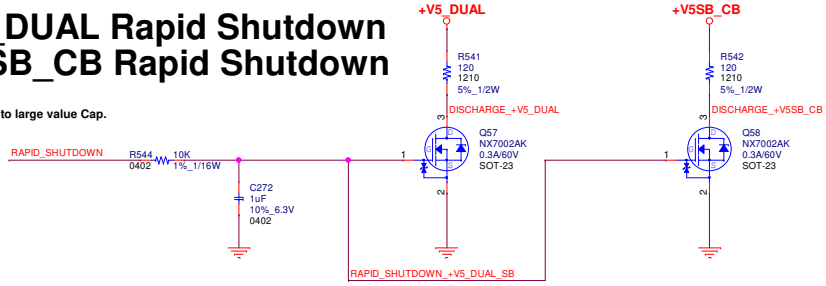
+V12 Rapid Shutdown

CAD Note:
Place close to large value Cap.



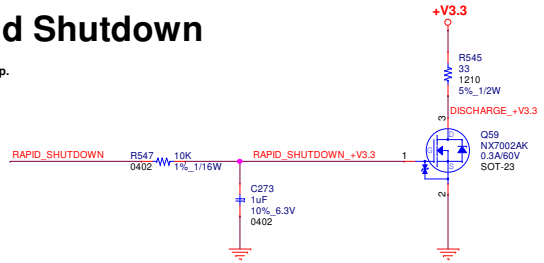
+V5_DUAL Rapid Shutdown
+V5SB_CB Rapid Shutdown

CAD Note:
Place close to large value Cap.



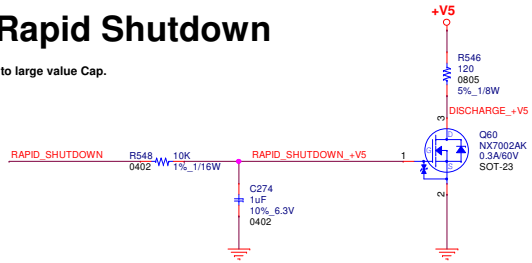
+V3.3 Rapid Shutdown

CAD Note:
Place close to large value Cap.



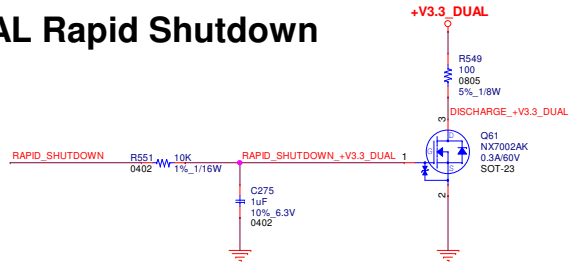
+V5 Rapid Shutdown

CAD Note:
Place close to large value Cap.



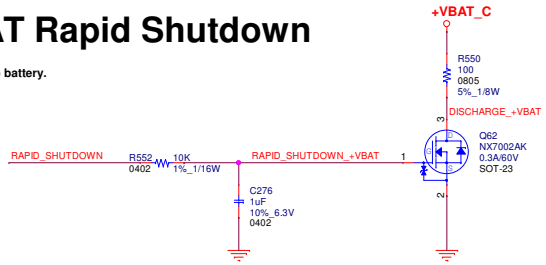
+V3.3_DUAL Rapid Shutdown

CAD Note:
Place close to large value Cap.



+VBAT Rapid Shutdown

CAD Note:
Place close to battery.



ADVANTECH

Title	RAPID SHUTDOWN	
Size	Document Number SOM-DB5830	Rev A1
Date: Monday, October 22, 2018	Sheet 28 of 34	

SOM-DB5830 A1 01-1 PCB:19A6583000-01, 96 BOM:96965830000 Date: 2017/10/13

SOM-DB5830 A1 01-2 PCB:19A6583001-01, 96 BOM:96965830000 Date: 2018/03/26

PG21: R519 need to mount for BUZZER function.

PG20: Change SMART_FAN1 from 1655004909-01 to 1655004347 for common part.

PG27: Add C1142 & C1165 for +VIN low voltage power ripple.

PG17: Change component at PG17 for LVDS sequence.

PG18: Correct name error from SW_HMDI_EQ1 to SW_HDMI_EQ1.

PG04: change J1 from 1653006504-01 to 1653002200 for duplicated part.

PG20: Update SMART_FAN1 PIN4 FANPWM schematic.

PG20: Change C202 from 0.1uF to 0.01uF for FANTACH waveform abnormal.

PG24: Update COM1 of Q28 schematic for connect mistake.

PG24: Change R475 to 2k and R481 to 1k for CAN_TX waveform abnormal.

PG11: Change SATA1~SATA4 from 1654005955 to 1654013393-01 for DFM request.

PG11: Update schematic for two SPI BIOS ROM support.

PG11: Add J3(1-2) jumper for two SPI BIOS ROM support.

PG21: Add SD_PWR_EN to CN1 PIN A86 to control SD CONN PWR.

PG26: Add schematic for TYPE2# & TYPE0# select.

PG15: Swap U7 SMB_M_CLK and SMB_M_DAT for connect mistake.

PG17: Change R2033 from +V3.3 to +V5_DUAL for +VLVDS_PANEL_PWR discharge.

PG17: Change R2034 from 1.2Kohm to 52.3ohm for +VLVDS_PANEL_PWR discharge.

PG23: Change TPM(U19) from 1410028322-01(FW5.61) to 1410028322-11(FW5.62).

PG23: Change R459 from 33k to 4.7k for FAE recommend.

PG23: Change LPC_PH1 from 1653007220 to 1653007270-01 for DFM request.

PG17: Reserve cap at LVDS signals for SI and remove Common Mode Choke.

PG09: Change HW Strap setting of equalization and flat gain for USB3.1 GEN2 TX.

PG21: Change Q27 from 1310390410-02 to 1310390410 for duplicated part.

PGXX: Change 2N7002 from 1315700214 to 1315700214-01 for part shortage issue.

PG06: Reserve Common Mode Choke co-layout for USB3.1 RX Port 0/1 signal.

PG07: Reserve Common Mode Choke co-layout for USB3.1 RX Port 2/3 signal.

PG10: Change USB20 port 4~7 Common Mode Choke from 1212003587-01 to 1212001302.

PG06: Change USB20 port 0/1 Common Mode Choke from 1212003587-01 to 1212001302.

PG07: Change USB20 port 2/3 Common Mode Choke from 1212003587-01 to 1212001302.

PG10: Change USB20 CONN USB2.0_1 from 1654012279-01 to 1654009643.

PG29: Change C84/C85/C88/C89 from X7R 4.7uF 10% 10V SMD 0805 to
X5R 4.7uF 10% 25V SMD 0603 for capacitance shortage issue.

PG17: Unmount C155 for LVDS sequence.

PG28: Change Q54 from 1315700210-04 to 1310006311-01 for clear CMOS issue.

SOM-DB5830 A101-3 PCB:19A6583002-01, 96 BOM:96965830000 Date: 2018/10/03

PG6: Change re-driver USB3.1 port 0/1.

PG7: Change re-driver USB3.1 port 2/3.

PG8: Change re-driver USB3.1 port 0/1.

PG9: Change re-driver USB3.1 port 2/3.