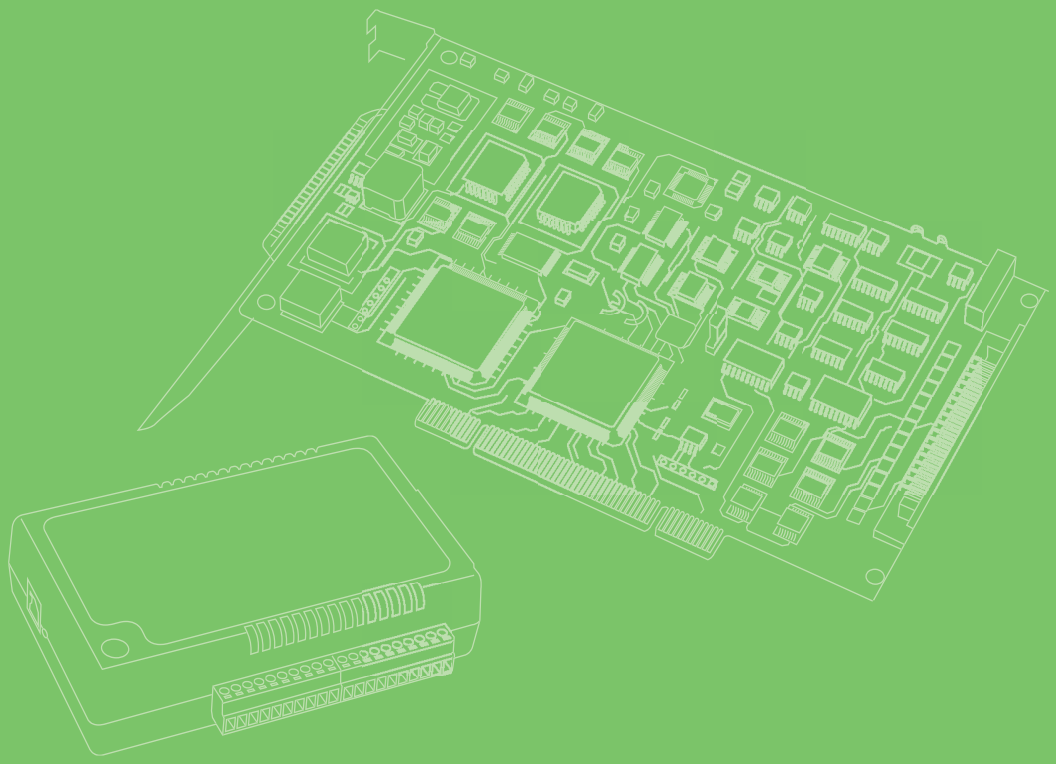

User Manual

PCIE-1810

12-bit Multifunction Card with PCI Express Bus

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2003181011 Edition 2

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the user manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In this event, users are required to correct the interference at their own expense.

Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that if not observed can cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage and data losses. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20 °C (-4 °F) or above 60 °C (140 °F) as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Contents

Chapter 1

Start Using PCIE-1810

1.1 Product Overview

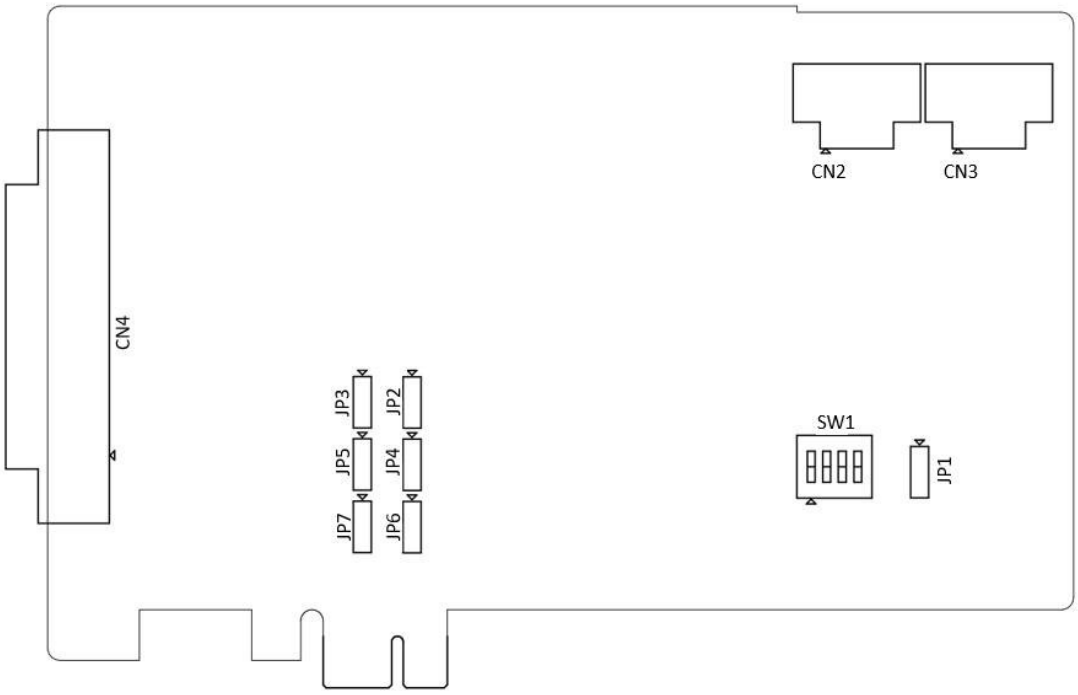

Figure 1.1 Card Layout

Table 1.1: List of connectors and switches

Component	Function
SW1	Board ID
CN2	MDSI IN
CN3	MDSI OUT
CN4	D-SUB 62-pin Connector
JP1	Power-on Configuration.
JP2 ~ JP7	DI/O Control Selection

1.2 Products Features

1.2.1 Board ID

A board ID can be assigned through the onboard slide switch for the device. The board ID value in the device description of the software is used to map the device in the software to the actual hardware device. Board ID is useful when there are multiple hardware devices with the same model name in the system. Without the board ID, user cannot recognize which device in the software that the hardware device is related to.

When configured as 0, the board ID is automatically assigned by the device driver software. When configured as value other than 0, the configured value is used. Do not configure the same value (except for 0) for hardware devices with the same model name. Refer to the device specifications for the configuration of the board ID.

If changed, the new board ID value takes effect only after cold resetting the device.

1.3 Driver Installation

The driver package could be found on Advantech Support Portal. Search for PCIE-1810 on the support portal, then the corresponded driver/SDK package could be found. You'll get the XNavi installer after the download session finishes.

Execute the installer, then it will guide you through the session. You can choose the device and software components you'd like to install in the system (Figure 1. 2). After the selection, click on "start" to begin the installation.

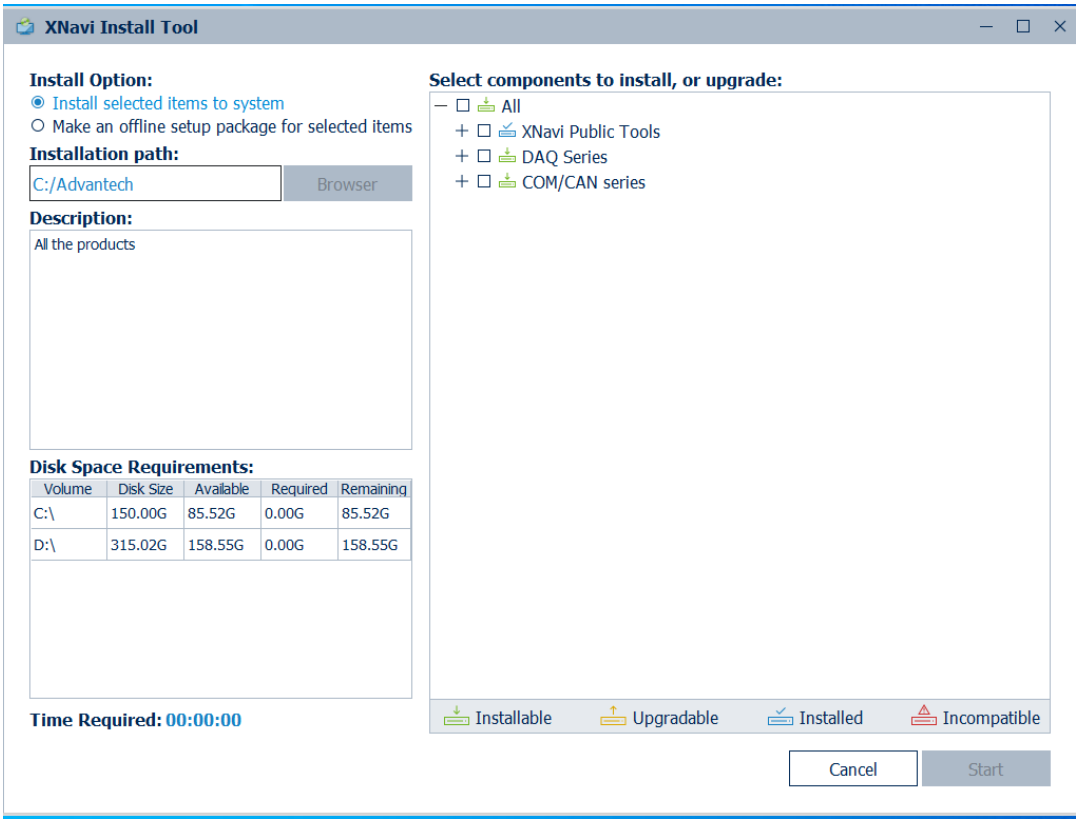

Figure 1.2 XNavi Installation Interface

1.4 Software Utility

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your DAQ devices. All these software packages are available on Advantech website: http://www.advantech.com/.

The Advantech Navigator is a utility that allows you to set up, configure and test your device, and later stores your settings in a proprietary database.

1. To set up the I/O device for your card, you could first run the Advantech Navigator program (by accessing Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator). The settings could also be saved.
2. You can then view the device(s) already installed on your system (if any) on the Installed Device tree view. If the software and hardware installation are completed, you will see DAQ devices in the Installed Devices list.

1.5 Software Development Using DAQNavi SDK

DAQNavi SDK is the software development kit for programming applications with Advantech DAQ products. The necessary runtime DLL, header files, software manual and tutorial videos can be installed via the XNavi installer. They can be found under C:\Advantech\DAQNavi (default directory) after finishing the installation.

1.6 FPGA Code Updates

The FPGA can also be updated via the interface in Navigator. However, it is not advised to update FPGA without first doing some research. Advantech strongly suggests you consult your technical support before starting an FPGA update.

Chapter 2

Installation Guide

2.1 Initial Unpacking Check

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- PCIE-1810 card
- Startup or User Manual

2.2 Hardware Installation and Configuration

2.2.1 Installation

Before you install your PCIE-1810, please make sure you have the following components:

- PCIE-1810 card
- PCIE-1810 User Manual
- Advantech DAQNavi SDK and the corresponding device driver
- Personal computer or workstation with PCI Express interface
- Accessories (optional)
  - 1700030423-01 10-pin flat cable for MDSI synchronization, 10 cm
  - PCL-10168H-1E 68-pin SCSI shielded cable with noise rejection, 1 m
  - PCL-10168H-2E 68-pin SCSI shielded cable with noise rejection, 2 m
  - PCL-10168-1E 68-pin SCSI shielded cable, 1 m
  - PCL-10168-2E 68-pin SCSI shielded cable, 2 m
  - ADAM-3968-AE 68-pin DIN rail SCSI wiring board

When the necessary components are prepared, you can begin the installation procedure as follows:

1. Install Advantech DAQNavi SDK and the corresponding device driver. They can be downloaded from Advantech website.
2. Turn off the computer. (for PCI or PCIe cards only)
3. Install the hardware device.
4. Turn on the computer. (for PCI or PCIe cards only)
5. Use Navigator to test the functionality of the hardware.
6. Read software manual and examples.
7. Write your own applications.

2.2.2 Configuration - Board ID (SW1)

Table 2.1: Configuration - Board ID (SW1)

Board ID	Switch Position			
	1	2	3	4
0*	UP	UP	UP	UP
1	UP	UP	UP	DOWN
2	UP	UP	DOWN	UP
3	UP	UP	DOWN	DOWN
4	UP	DOWN	UP	UP
5	UP	DOWN	UP	DOWN
6	UP	DOWN	DOWN	UP
7	UP	DOWN	DOWN	DOWN
8	DOWN	UP	UP	UP
9	DOWN	UP	UP	DOWN
10	DOWN	UP	DOWN	UP
11	DOWN	UP	DOWN	DOWN
12	DOWN	DOWN	UP	UP
13	DOWN	DOWN	UP	DOWN
14	DOWN	DOWN	DOWN	UP
15	DOWN	DOWN	DOWN	DOWN

2.2.3 Configuration - DI/O Control Selection (JP2 ~ JP7)

Table 2.2:

Jumper Setting	Description
	Software configurable.*
	Force output.

* Default setting.

Table 2.3:

Jumper Number	Relative channels
JP2	DIO 0-3
JP3	DIO 4-7
JP4	DIO 8-11
JP5	DIO 12-15
JP6	DIO 16-19
JP7	DIO 20-23

* Default setting.

2.3 Signal Connection and Pin Assignment

2.3.1 Analog Input Signal Connection

An analog input channel measures the voltage (VS) of the external source. Each two channels, for example, AI0 and AI1, AI2 and AI3, etc., can be configured as a differential input channel, or as two separate single-ended channels. When configured as a differential channel, even number channel is the positive terminal, and odd number channel is the negative terminal. When configured as separate single-ended channels, voltage should be applied between channel terminal and analog ground (AGND) terminal.

The voltage is routed through an analog multiplexer (MUX), amplified or attenuated by a programmable gain instrumentation amplifier (PGIA), and sampled and converted into a digital form of data by an analog-to-digital converter (ADC). Each channel is converted by the ADC in channel by channel order. That is, only one channel at a time is being converted. This architecture is called multiplexed analog input. Analog input signal connection and internal functional block diagram is shown in Figure 2. 1.

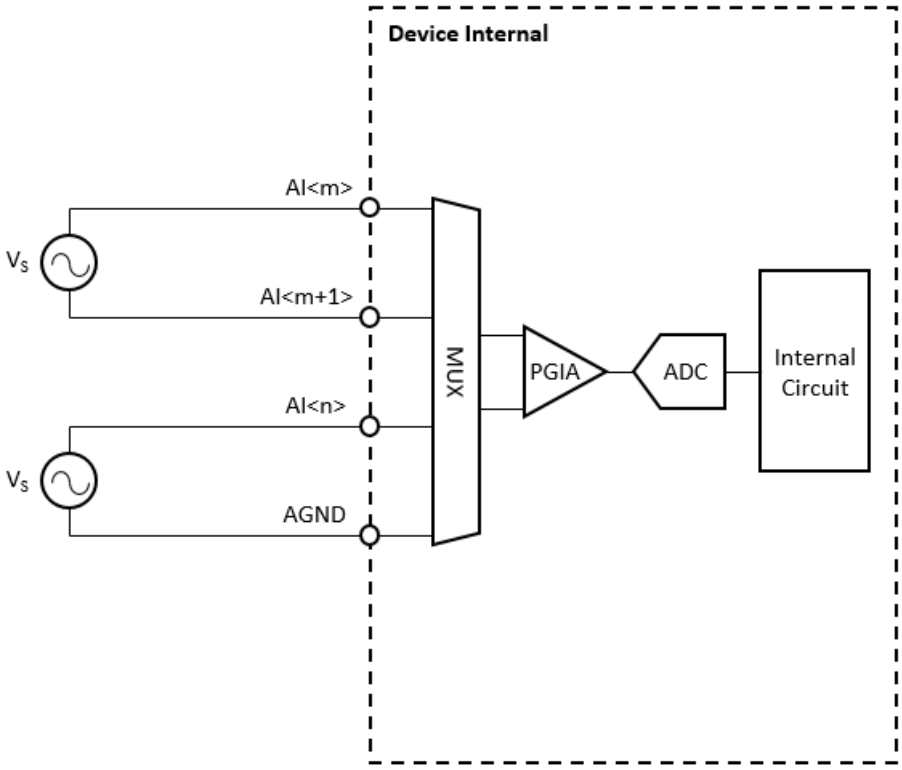

Figure 2.1 Analog input signal connection

2.3.2 Analog Output Signal Connection

An analog output channel generates a voltage output to the load. The voltage to be generated is first sent by the internal controller to the digital-to-analog converter (DAC) in a form of digital data, and the data is converted by the DAC to an analog output voltage. The analog output channel is of single-ended type, hence the load should be connected between the analog output (AO) terminal and the analog ground (AGND) terminal. This is shown in Figure 2. 2

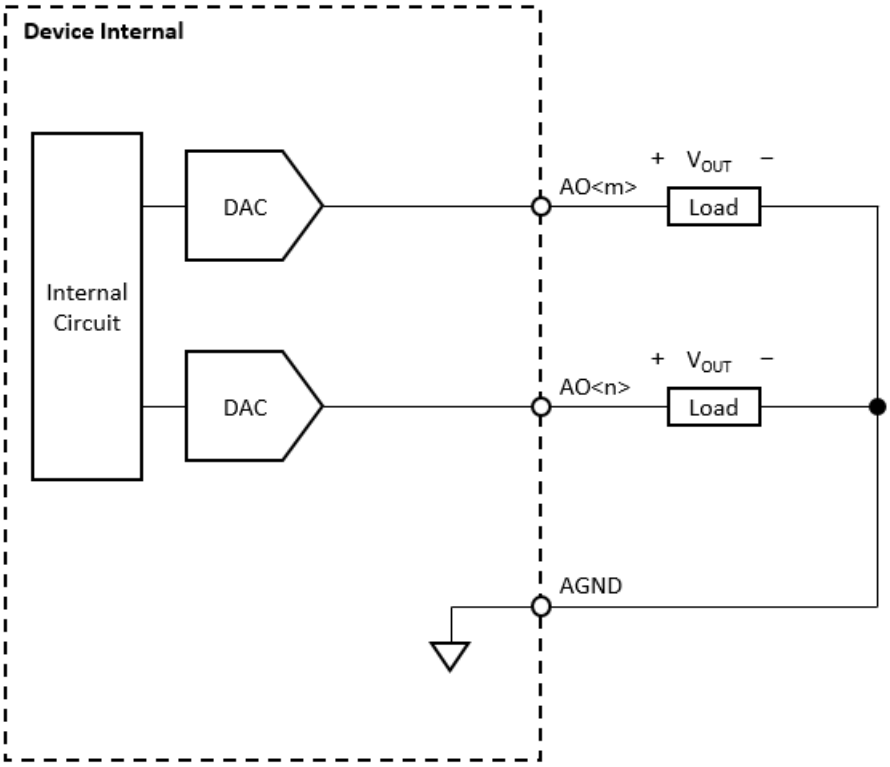

Figure 2.2 Analog output signal connection

Multiple output ranges are supported and can be selected by software for each channel independently. Be sure that the load resistance is within the range of the device specifications, or the output voltage may not reach the specified value due to the limitation of output driving capability.

The output range can also be defined by an external reference voltage which is connected to the analog output reference (AO_REF) terminal. Refer to the device specifications for the relationship between the output range and the external reference voltage. In this configuration, however, the output voltage is not calibrated, and the accuracy of the output voltage depends on the accuracy of the external reference voltage. Users can perform calibration through the calibration utility in the Advantech Navigator by themselves.

2.3.3 Trigger Input Signal Connection

The trigger can come from one of various signal sources. If the signal source is of digital type (logic high or low), it is called a digital trigger. On the other hand, if the signal source is of analog type (voltage level), it is called an analog trigger.

Digital Trigger

A digital trigger can be configured as rising edge active or falling edge active, as shown in Figure 2. 3, Figure 2. 4 respectively.

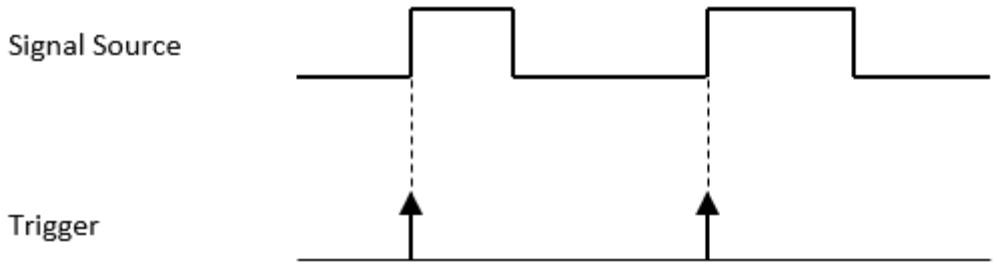

Figure 2.3 Rising edge active digital trigger

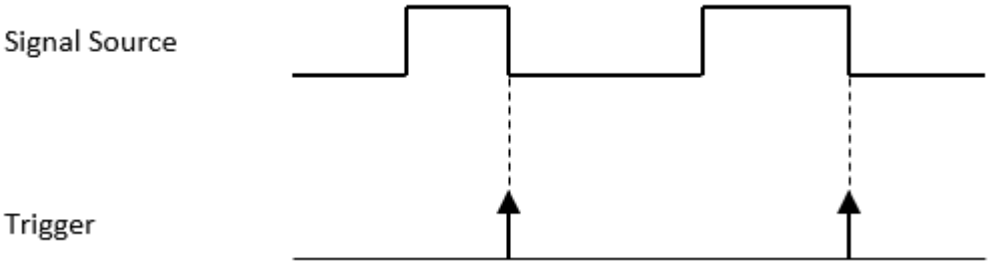

Figure 2.4 Falling edge active digital trigger

Analog Trigger

In addition to active edge, user can configure the threshold level and the hysteresis value for an analog trigger. The threshold level specifies the analog input voltage level where the trigger occurs. The hysteresis value prevents unwanted triggers due to noisy signals.

A rising edge active analog trigger occurs when the signal crosses the threshold level from below. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level minus the hysteresis value from above before it crosses the threshold level from below again. This is shown in Figure 2. 5.

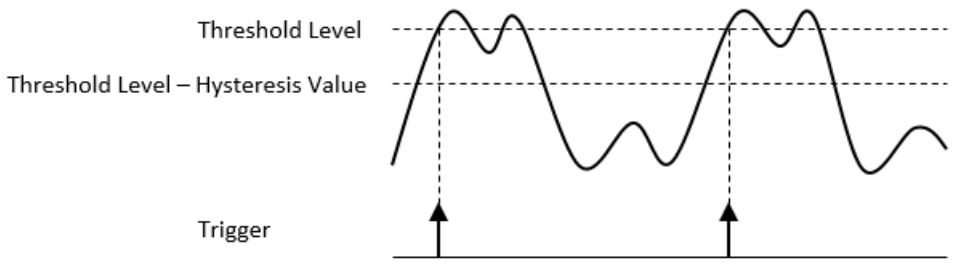

Figure 2.5 Rising edge active analog trigger

A falling edge active analog trigger occurs when the signal crosses the threshold level from above. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level plus the hysteresis value from below before it crosses the threshold level from above again. This is shown in Figure 2. 6.

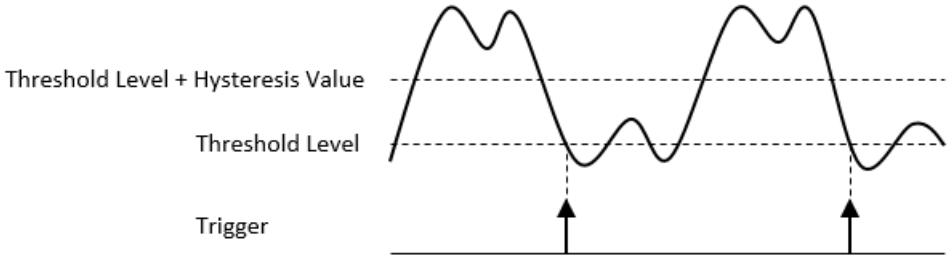

Figure 2.6 Falling edge active analog trigger

2.3.4 Digital Input Signal Connection

A digital input/output (DI/O) channel can be configured by software to perform digital input measurement, which is the power-on default configuration, or digital output generation. When performing digital input measurement, the voltage logic level between the digital input (DI) terminal and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the digital input channel can be configured as internally pulled-up or pulled-down by software. This is shown in Figure 2. 7.

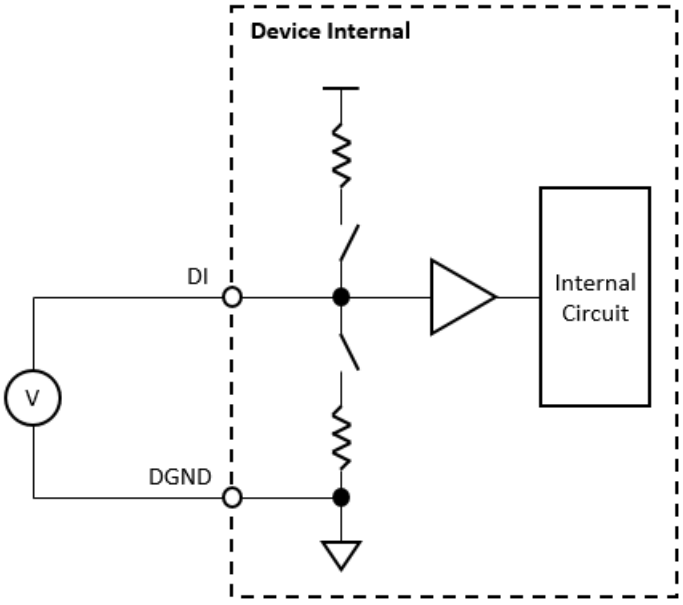

Figure 2.7 Digital input signal connection

The input voltage must be either higher than the minimum value of ON state or lower than the maximum value of OFF state for deterministic result. If the input voltage is between these two values, the result is undetermined, which may be ON or OFF. In addition, do not input a voltage higher than the maximum allowable value of ON state or lower than the minimum allowable value of OFF state. The device may be damaged under such circumstance. Refer to the device specifications for ON and OFF state voltage ranges.

The digital input channel can also sense the status of an external switch. When configured as internally pulled-up, the status of an external switch which is connected

between the DI terminal and the DGND terminal is sensed as shown in Figure 2. 8. When configured as internally pulled-down, the status of an external switch which is connected between the external source and the DI terminal is sensed as shown in Figure 2. 9. Be sure the voltage of the external source is within the allowable range of ON state as specified in the device specifications.

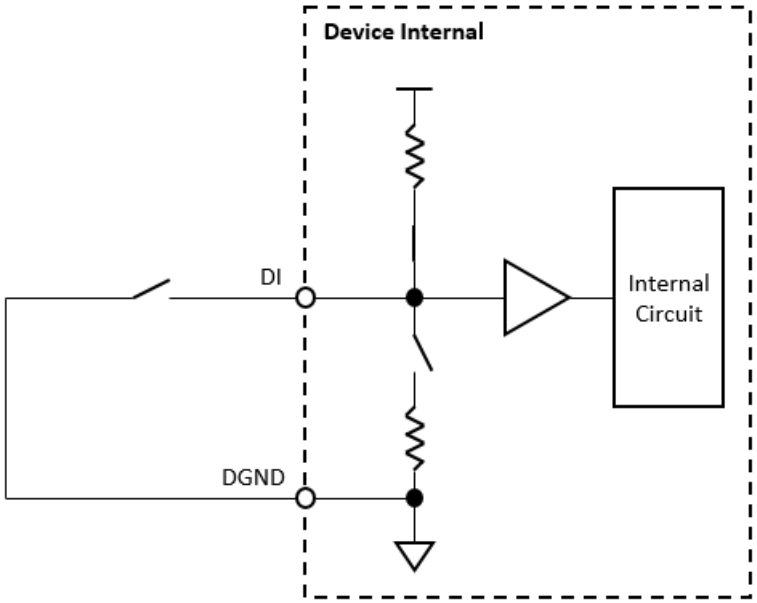

Figure 2.8 Digital input signal connection using a switch with internally pulled-up

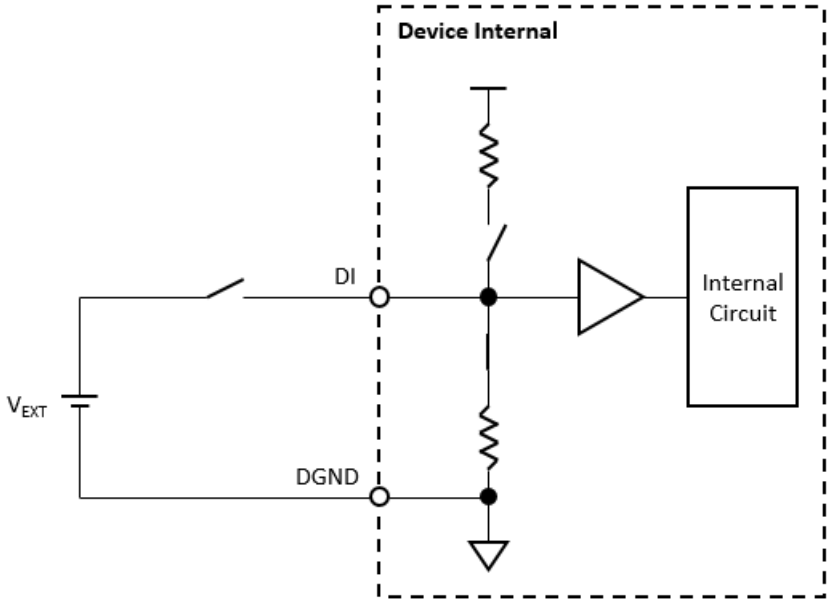

Figure 2.9 Digital input signal connection using a switch with internally pulled-down

2.3.5 Digital Output Signal Connection

A digital input/output (DI/O) channel can be configured by software to perform digital input measurement, which is the power-on default configuration, or digital output generation. When performing digital output generation, a voltage logic level is generated between the digital output (DO) terminal and the digital ground (DGND) terminal. This is shown in Figure 2. 10.

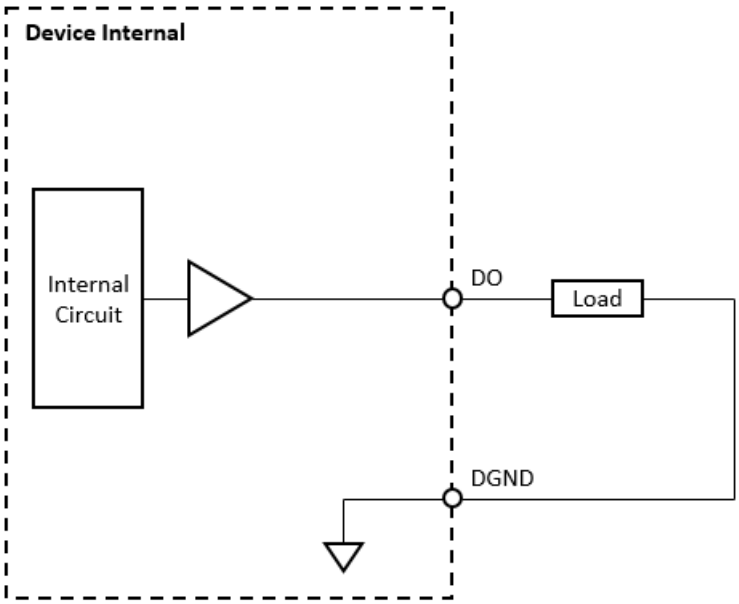

Figure 2.10 Digital output signal connection

Each digital output channel can source or sink only finite amounts of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and sink current values.

2.3.6 Counter Input Signal Connection

The voltage logic level between the counter input (counter clock, counter gate, counter arm, and sample clock) terminals and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the counter input signals are internally pulled-up. This is shown in Figure 2. 11.

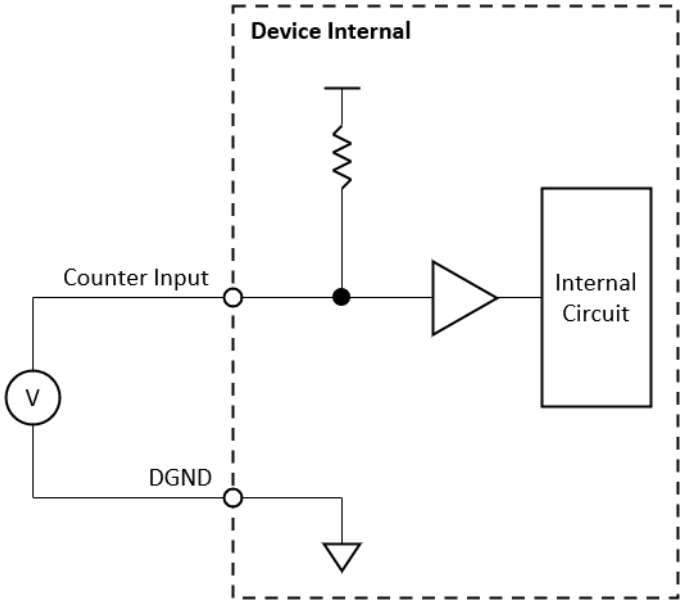

Figure 2.11 Counter input signal connection

For a deterministic outcome, the input voltage should either surpass the minimum ON state value or fall below the maximum OFF state value. If the input voltage lies between these thresholds, the result becomes indeterminate, leading to either an ON or OFF state. Moreover, avoid supplying a voltage exceeding the maximum allowed ON state value or going below the minimum allowed OFF state value, as it may damage the device. Refer to the device specifications for the specified voltage ranges in the ON and OFF states.

The counter input signals can also sense the status of an external switch. The status of an external switch which is connected between the counter input terminals and the DGND terminal is sensed as shown in Figure 2. 12.

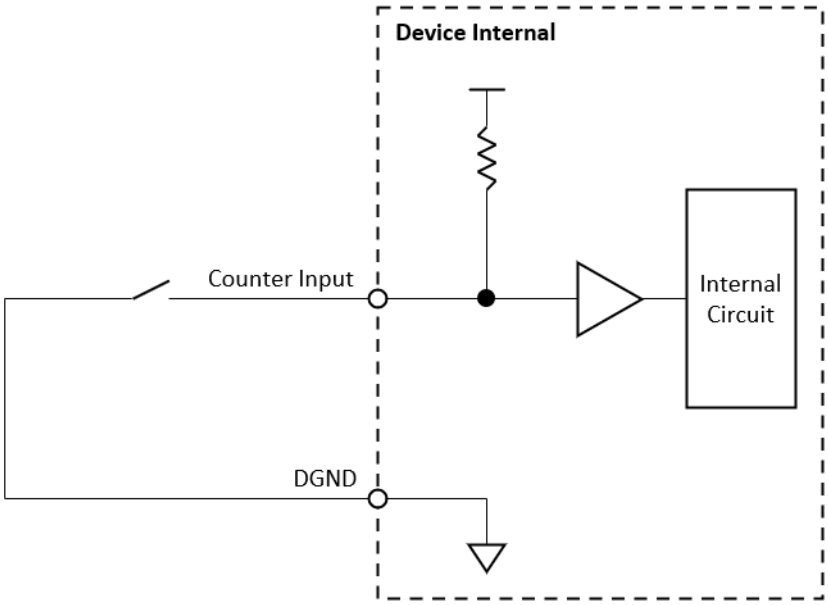

Figure 2.12 Counter input signal connection using a switch with internally pulled-up

2.3.7 Counter Output Signal Connection

A voltage logic level is generated between the counter output terminal and the digital ground (DGND) terminal. This is shown in Figure 2. 13.

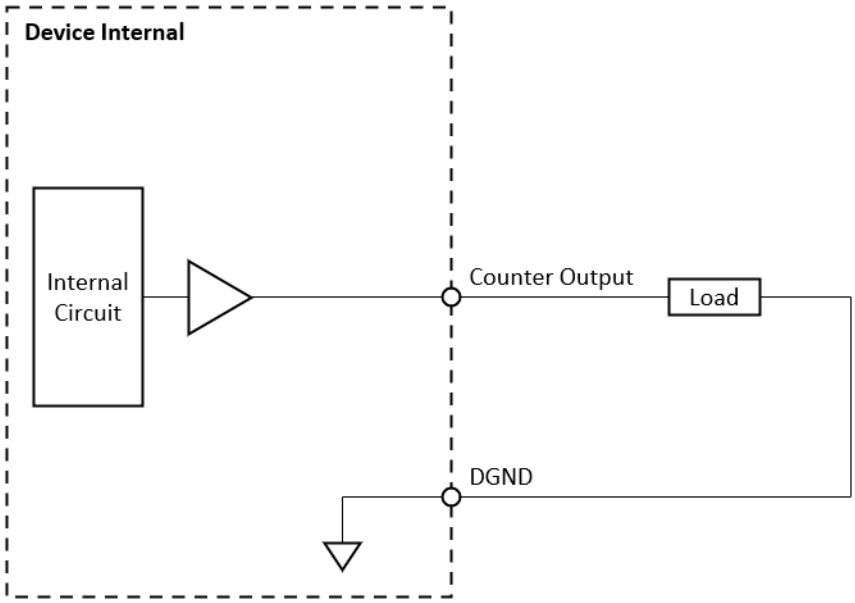

Figure 2.13 Counter output signal connection

Each counter output channel can source or sink only a finite amount of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and sink current values.

2.3.8 Pin Assignment (CN4)

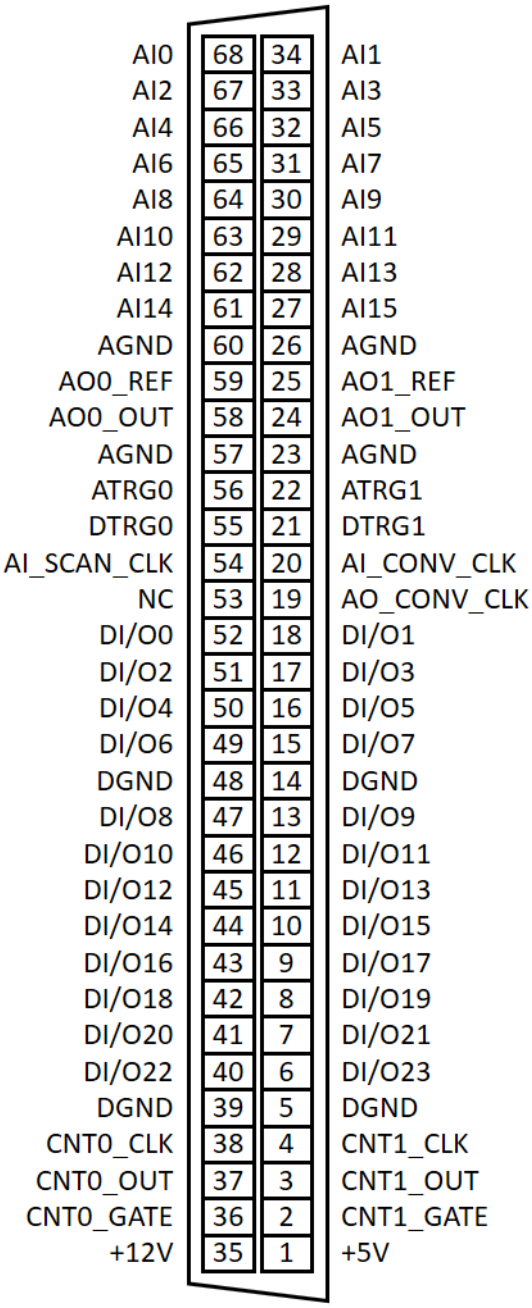

Figure 2.14 Pin assignment

Table 2.4: Pin assignment

Pin Name	Direction	Description	Pin Number
AI<0..15>	I	Analog input terminals. Each channel pair (AI0 & AI1, AI2 & AI3, etc.) can be configured as a differential input channel or two single-ended channels.	27 ~ 34, 61 ~ 68
AO<0..1>_REF	I	Analog output reference voltage input terminals.	25, 59
AO<0..1>_OUT	O	Analog output terminals.	24, 58
ATRG<0..1>	I	Analog trigger input terminals.	22, 56
AGND	-	Ground terminals for analog signals.	23, 26, 57, 60
DTRG<0..1>	I	Digital trigger input terminals.	21, 55
AI_SCAN_CLK	I	Analog input scan clock.	54
AI_CONV_CLK	I	Analog input conversion clock.	20
AO_CONV_CLK	I	Analog output conversion clock.	19
NC	-	Not connected terminal.	53
DI/O<0..15>	I/O	Digital input/output terminals.	6 ~ 13,15 ~ 18, 40 ~ 47,49 ~ 52
CNT<0..1>_CLK	I	Counter clock input terminals.	4, 38
CNT<0..1>_OUT	O	Counter output terminals.	3, 37
CNT<0..1>_GATE	I	Counter gate input terminals.	2, 36
DGND	-	Ground terminals for digital signals.	5, 14, 39, 48
+12V	O	+12 V supply output.	35
+5V	O	+5 V supply output.	1

2.4 Grounding Considerations

2.4.1 Signal Source Type

Signal sources can be categorized as grounded (ground-referenced) signal source or ungrounded (floating) signal source. This is shown in Figure 2. 15.

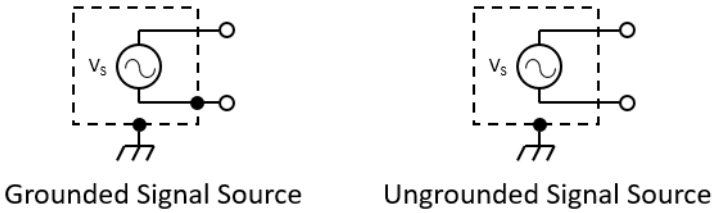

Figure 2.15 Signal source type

The voltage of a grounded signal source is referenced to a system ground, such as earth or building ground. That is, the negative terminal of the signal source is connected to the system ground. Examples of grounded signal source are devices that are plugged into the building ground through a wall outlet. The grounds of two independently grounded devices may not be at the same potential.

An ungrounded signal source is that in which the voltage is not referenced to a system ground. Examples of grounded signal source are battery powered devices, thermocouples, and isolated devices.

2.4.2 Measuring a Grounded Signal Source

To measure a grounded signal source from a grounded signal source, it is advisable to employ a differential input configuration. As explained earlier, the grounds of two devices both grounded may not share the same potential. If a single-ended (grounded) input configuration is utilized for measuring a grounded signal source, a ground loop is established, leading to current flow between the two grounds. This current flow produces common-mode noise during the measurement. This is shown in Figure 2. 16.

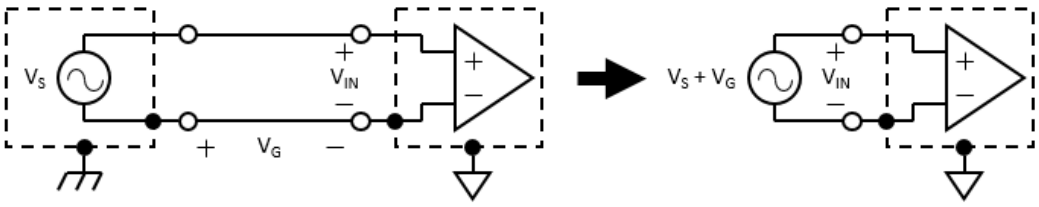

Figure 2.16 Ground loop effect

If differential (ungrounded) input configuration is used instead, the high input impedance of the negative input terminal prevents ground loop current from flowing, and therefore rejects the common-mode noise.

2.4.3 Measuring an Ungrounded (Floating) Signal Source

For an ungrounded (floating) signal source, both differential input configuration and single-ended input configuration are suitable. When using differential input configuration, however, care must be taken to ensure the input common-mode voltage level remains in the allowable range of the measuring device. Due to the lack of DC path to the ground, the input bias current of input stage amplifier may move the common-mode voltage level of the ungrounded signal source out of the allowable range of the measuring device. When this happens, the measured result will be incorrect or saturated (positive full-scale or negative full-scale). Resistors with equal resistance value connecting between each input terminal and ground can be used to alleviate this issue as shown in Figure 2. 17. These resistors are called bias resistors.

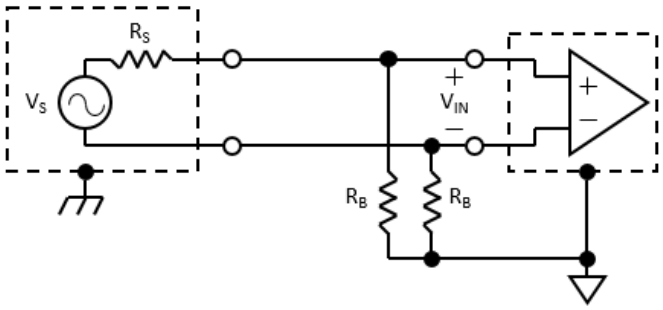

Figure 2.17 Differential input configuration with bias resistors

The resistance value should be large enough that it does not load the signal source and keep it remain floating, but small enough to make input common-mode voltage level stay in the allowable range. Typically, resistance value between 10 kΩ to 100 kΩ work well with low-impedance sources such as thermocouples and signal conditioning module outputs. When using bias resistor, the measured voltage will be attenuated by the voltage divider formed by source resistance of the signal source and bias resistors. This is shown in the following equation.

$$V_{IN} = \frac{2 \times R_B}{R_S + 2 \times R_B} V_S$$

If the source impedance of the signal source is low, only one resistor connecting between the negative input terminal and the ground is required to prevent input common-mode voltage level issue. However, this will lead to an unbalanced system if the source impedance is relatively high. A balanced system is desirable from a noise immunity point of view.

2.5 Field Wiring Considerations

When measuring a signal using the device, noises in the environment might significantly affect the performance of the measurement if some precautions are not taken. Follow these recommendations to avoid degradation of the measurement result.

- Make signal lines as short as possible.
- Use shielded, twisted-pair cables.
- Keep signal lines from noisy environment, high-voltage/current cables, or equipment which generates large electromagnetic interference, such as power lines, motors, breakers, or welding equipment.
- Route signal lines at right angles to noise generating cables.
- Use differential input configuration to reduce common-mode noise.
- For externally powered modules, use separate power sources for modules and other noise generating equipment.

2.6 Board ID Configuration

The PCIE-1810 has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same chassis, this board ID switch is useful for identifying each card's device number.

Table 2.5: Board ID

Board ID	Switch Position			
	1	2	3	4
0*	UP	UP	UP	UP
1	UP	UP	UP	DOWN
2	UP	UP	DOWN	UP
3	UP	UP	DOWN	DOWN
4	UP	DOWN	UP	UP
5	UP	DOWN	UP	DOWN
6	UP	DOWN	DOWN	UP
7	UP	DOWN	DOWN	DOWN
8	DOWN	UP	UP	UP
9	DOWN	UP	UP	DOWN
10	DOWN	UP	DOWN	UP
11	DOWN	UP	DOWN	DOWN
12	DOWN	DOWN	UP	UP
13	DOWN	DOWN	UP	DOWN
14	DOWN	DOWN	DOWN	UP
15	DOWN	DOWN	DOWN	DOWN

Chapter 3

Functions Details

3.1 Analog Input

The device supports both instant (software-timed) and buffered (hardware-timed) analog input acquisitions.

3.1.1 Instant (Software-Timed) Analog Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current value of analog input channel is returned as shown in Figure 3. 1.

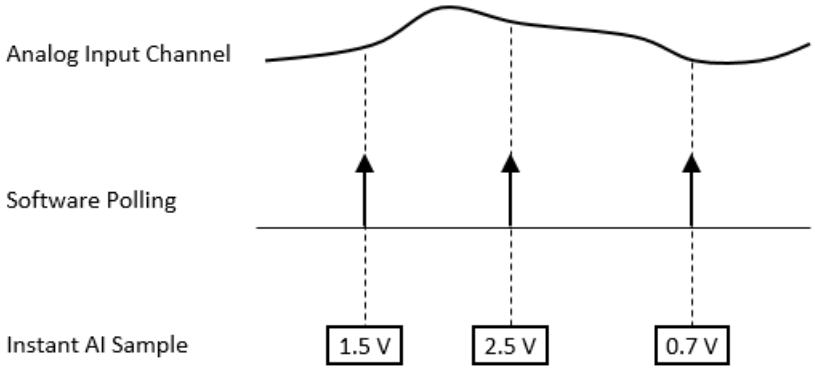

Figure 3.1 Instant (software-timed) analog input acquisition

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of analog input.

3.1.2 Buffered (Hardware-Timed) Analog Input Acquisition

With buffered acquisition, a hardware signal called conversion clock controls the rate and time of acquisition. The ADC begins to convert the analog input voltage at each rising edge of the conversion clock. After the ADC begins conversion, the analog multiplexer routes the next buffered acquisition enabled analog input channel to the ADC, which will be converted at the next rising edge of the conversion clock. Figure 3. 2 shows an example of analog input buffered acquisition which AI0, AI1, and AI2 are enabled.

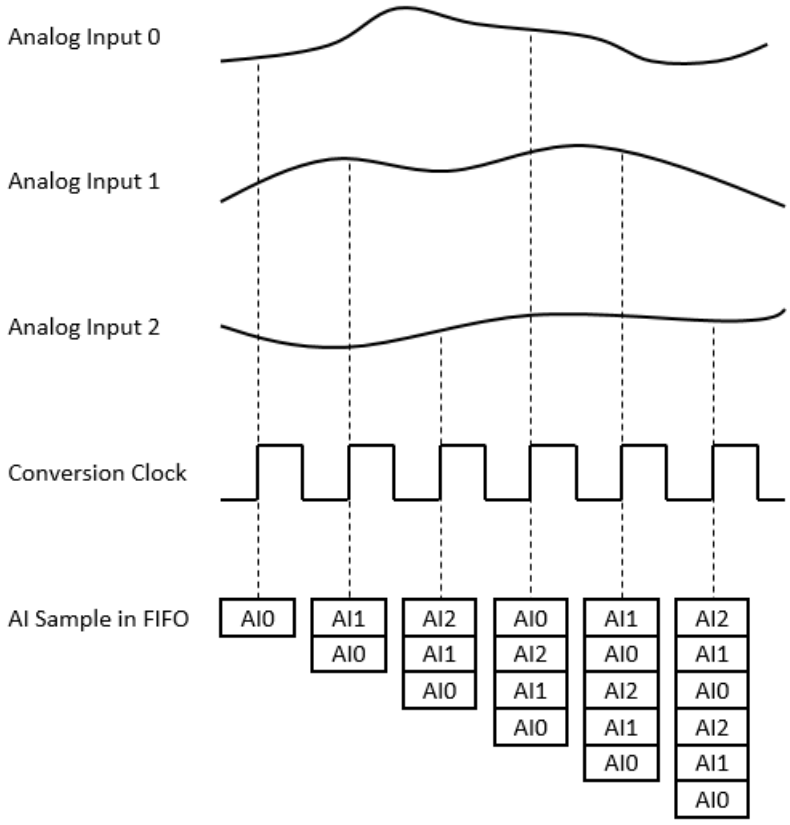

Figure 3.2 Buffered (hardware-timed) analog input acquisition

The conversion clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported conversion clock sources and the maximum allowable frequency of conversion clock.

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory of the device, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allows much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.2 Analog Output

The device supports both static (software-timed) analog output update and buffered (hardware-timed) analog output generation.

3.2.1 Static (Software-Timed) Analog Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the value of analog output channel is updated as shown in Figure 3. 3.

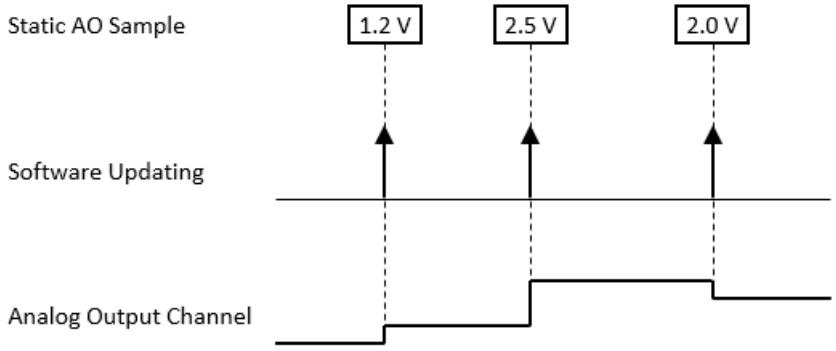

Figure 3.3 Static (software-timed) analog output update

State updates offer the benefit of low latency, making them ideal for writing a singular analog output value. In the case of updating multiple analog output channels, there are two approaches: asynchronous or synchronous. In asynchronous updating, each analog output channel is promptly updated as soon as the value is written to the device, as illustrated in Figure 3.4. On the other hand, synchronous updating involves storing the values to be updated in the device first. The update then occurs simultaneously for all analog output channels when the synchronous write command is issued. This is shown in Figure 3. 5.

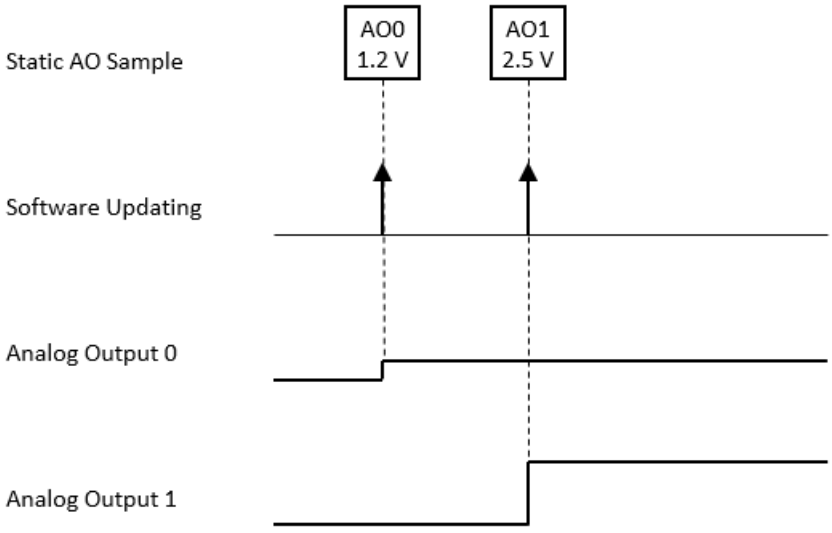

Figure 3.4 Analog output asynchronous update

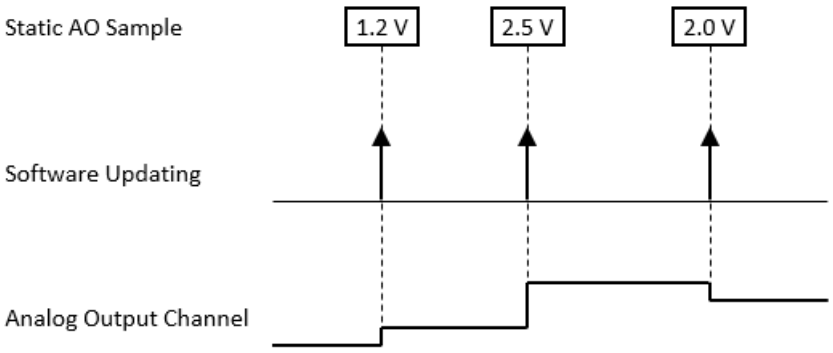

Figure 3.5 Analog output synchronous update

3.2.2 Buffered (Hardware-Timed) Analog Output Generation

With buffered generation, a hardware signal called a sample clock controls the rate and time of generation as shown in Figure 3. 6. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

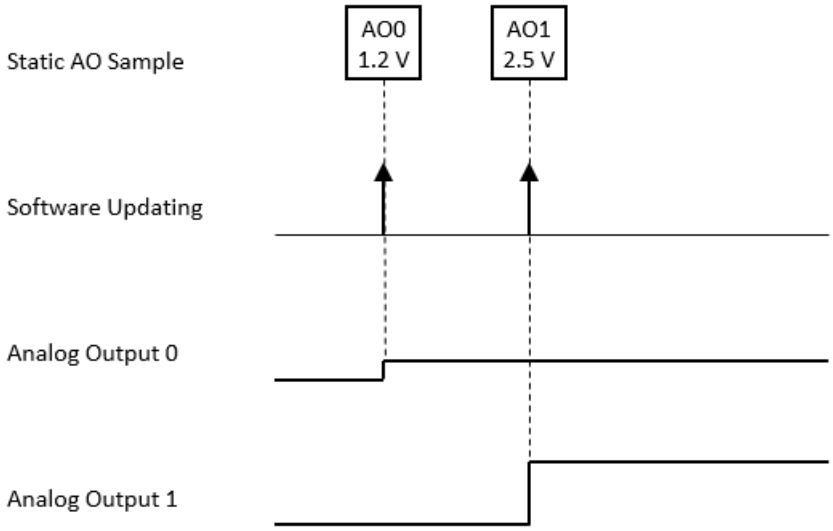

Figure 3.6 Buffered (hardware-timed) analog output generation

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the device by a direct memory access (DMA) engine, and converted by the DAC one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved in large blocks instead of one point at a time, buffered generation typically allows much higher transfer rates. Buffered generation is also called hardware-timed generation.

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.3 Digital Input

The device supports both instant (software-timed) and buffered (hardware-timed) digital input acquisitions.

3.3.1 Instant (Software-Timed) Digital Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current status of digital input ports is returned as shown in Figure 3. 7.

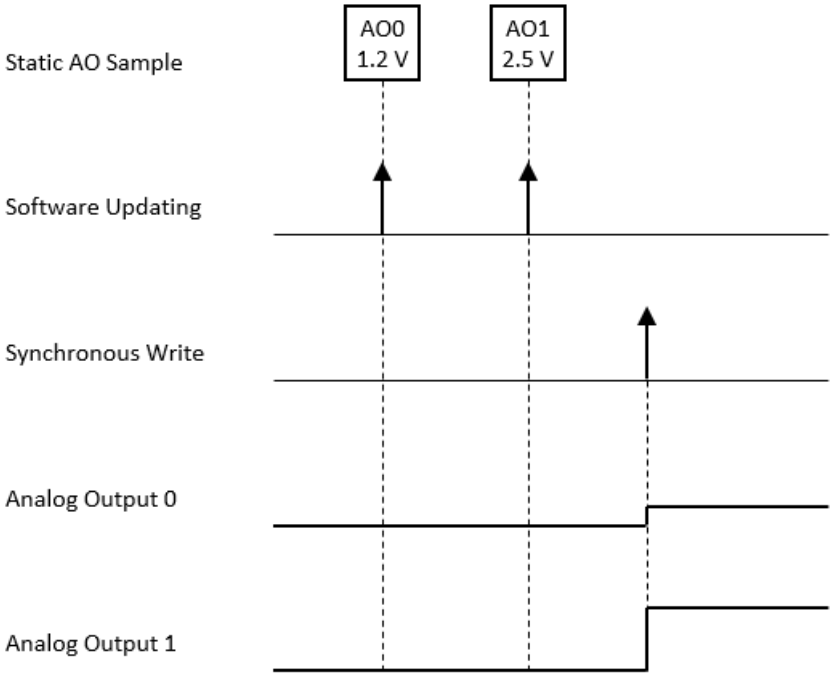

Figure 3.7 Instant (software-timed) digital input acquisition

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of digital input.

3.3.2 Buffered (Hardware-Timed) Digital Input Acquisition

With buffered acquisition, a hardware signal called a sample clock controls the rate and time of acquisition as shown in Figure 3. 8. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

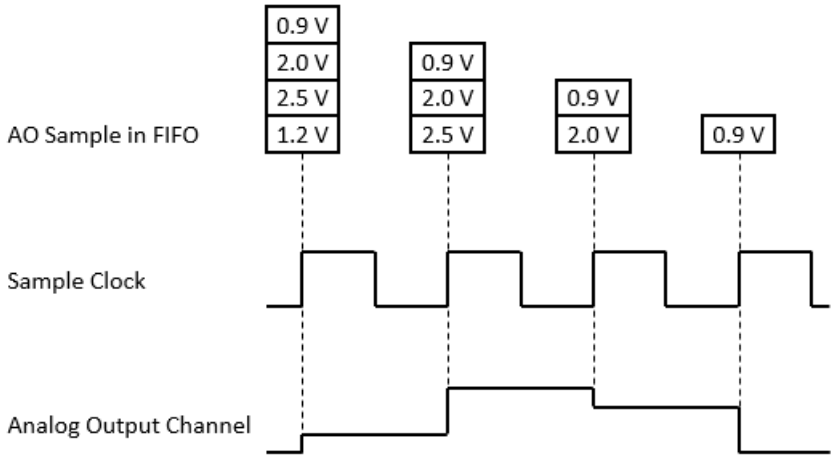

Figure 3.8 Buffered (hardware-timed) digital input acquisition

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory of the device, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allow much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.4 Digital Output

The device supports both static (software-timed) digital output update and buffered (hardware-timed) digital output generation.

3.4.1 Static (Software-Timed) Digital Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the state of digital output ports is updated as shown in Figure 3. 9.

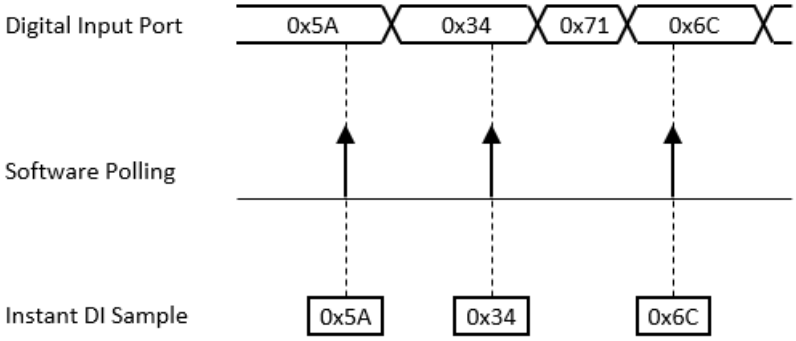

Figure 3.9 Static (software-timed) digital output update

The advantage of state update is low latency. It is typically used for writing a single value of digital output.

3.4.2 Buffered (Hardware-Timed) Digital Output Generation

With buffered generation, a hardware signal called sample clock controls the rate and time of generation as shown in Figure 3. 10 The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

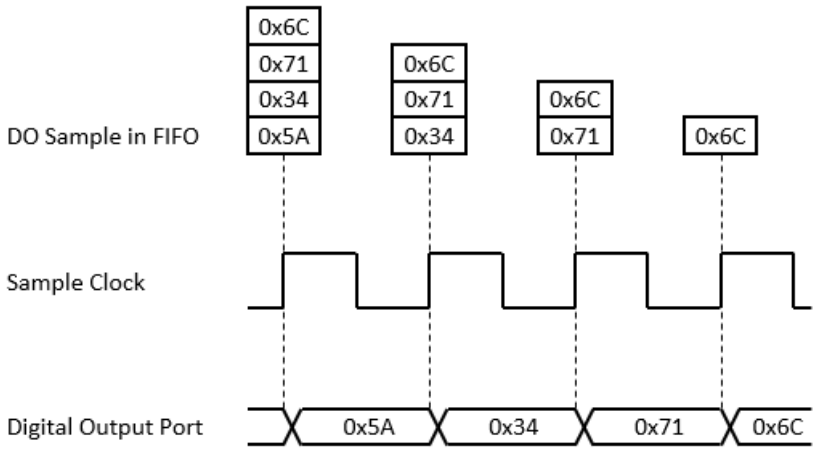

Figure 3.10 Buffered (hardware-timed) digital output generation

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the device by a direct memory access (DMA) engine, and placed on the digital output channels one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved

in large blocks instead of one point at a time, buffered generation typically allow much higher transfer rates. Buffered generation is also called hardware-timed generation.

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.5 Counter

3.5.1 Event Counting

In event counting mode, the counter counts the number of edges the counter clock signal generates. It can be configured as rising edge active or falling edge active, as shown in Figure 3. 11 and Figure 3. 12, respectively.

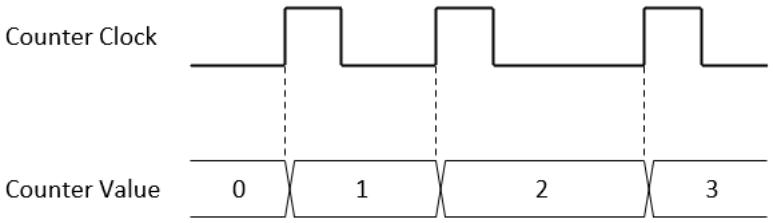

Figure 3.11 Rising edge event counting

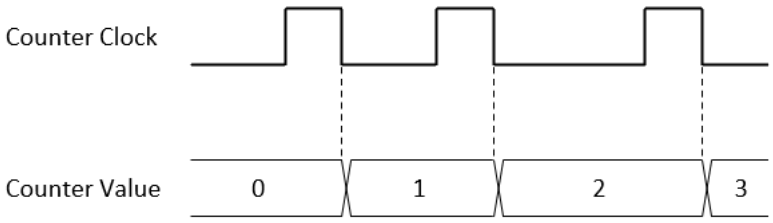

Figure 3.12 Falling edge event counting

Counting may be temporarily paused by the counter gate signal as shown in Figure 3. 13.

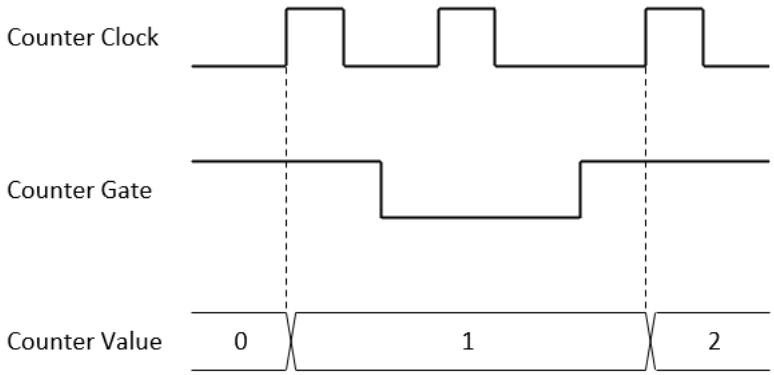

Figure 3.13 Event counting with pause gate

Instant (Software-Timed) Event Counting

With instant event counting, the software controls the rate and time of reading counter value, which is thus also called software-timed event counting. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3. 14.

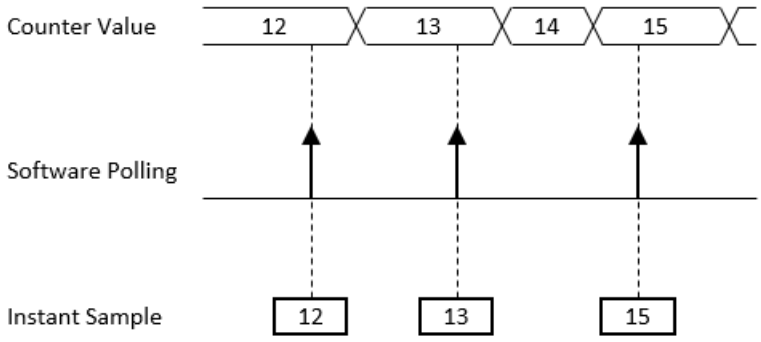

Figure 3.14 Instant (software-timed) event counting

The advantage of instant event counting is low latency. It is typically used for reading a single sample of counter value.

3.5.2 Frequency Measurement

In frequency measurement mode, the frequency of the counter clock signal is measured by one of the two measuring methods: Period inversion or counting number of pulses in fixed duration.

Period Inversion

In this method, the period of the counter clock signal is first measured by an internal high frequency clock. The frequency of the signal is then calculated by inverting the period value. This is shown in Figure 3. 15 and by the following equation.

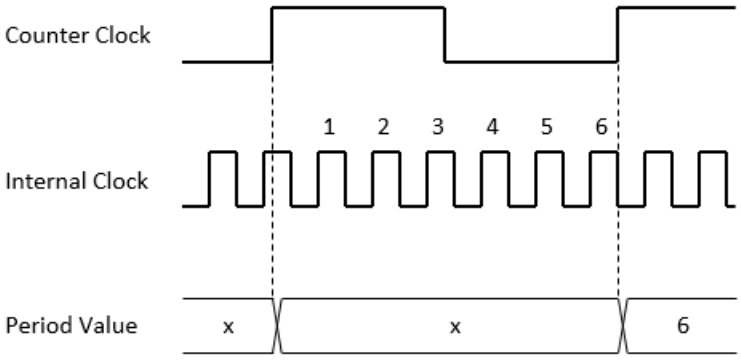

Figure 3.15 Frequency measurement by period inversion

$$Frequency = \frac{1}{Period} = \frac{1}{InternalClockCount \quad InternalClockPeriod}$$

This method is suitable if the counter clock signal frequency is much smaller (< 0.1%) than the internal clock frequency. Measuring accuracy degrades as the counter clock signal frequency increases.

Counting Number of Pulses in Fixed Duration

In this method, the pulse number of the counter clock signal is measured in a fixed time duration. The frequency of the signal is then calculated by dividing this number by the time duration. This is shown in Figure 3. 16 and by the following equation.

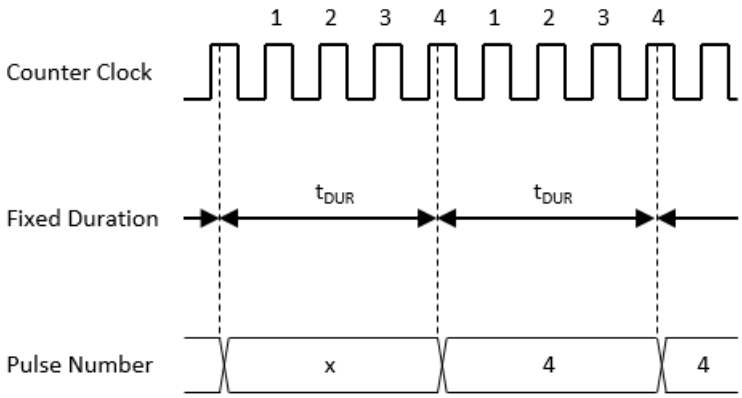

Figure 3.16 Frequency measurement by counting number of pulses in fixed duration

$$Frequency \quad \frac{PulseNumber}{t_{DUR}}$$

For counter clock signal frequency higher than that specified in the previous section, this method gives a more accurate result.

Instant (Software-Timed) Frequency Measurement

With instant frequency measurement, the software controls the rate and time of reading frequency value, which is thus also called software-timed frequency measurement. Whenever the software sends a read command, the current value of the frequency is returned as shown in Figure 3. 17.

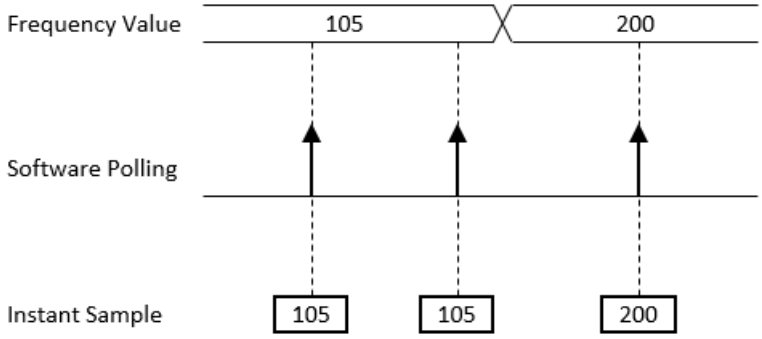

Figure 3.17 Instant (software-timed) frequency measurement

The advantage of instant frequency measurement is low latency. It is typically used for reading a single sample of frequency value.

3.5.3 Pulse Width Measurement

In pulse width measurement mode, both the high period and the low period of the counter clock signal are measured. The measured values are updated when a pulse is completed. This is shown in Figure 3. 18.

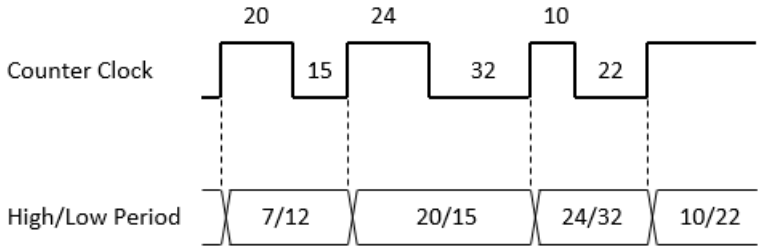

Figure 3.18 Pulse width measurement

Instant (Software-Timed) Pulse Width Measurement

With instant pulse width measurement, the software controls the rate and time of reading counter value, which is thus also called software-timed pulse width measurement. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3. 19.

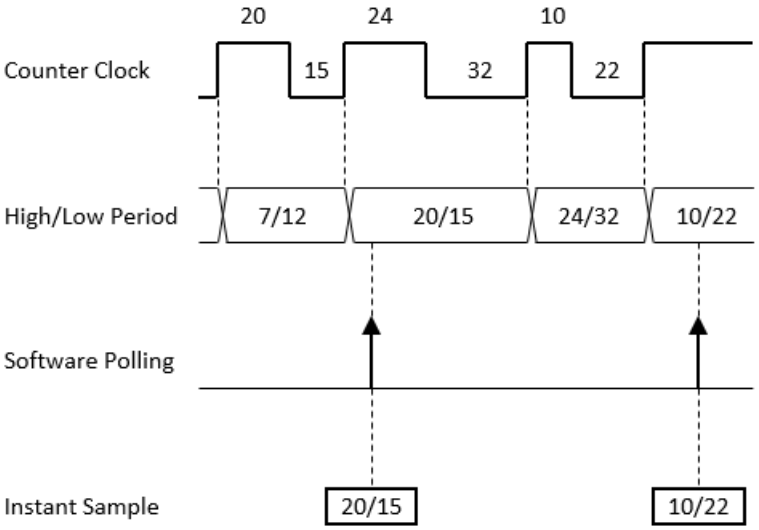

Figure 3.19 Instant (software-timed) pulse width measurement

The advantage of instant pulse width measurement is low latency. It is typically used for reading a single sample of the counter value.

3.5.4 One-Shot (Delayed Pulse Generation)

In one-shot mode, when an active edge of gate signal is detected, a pulse will be generated after the specified number source clock counts. The pulse width is one period of source clock. Figure 3. 20 shows an example of high-pulse, 5-clock delay one-shot output.

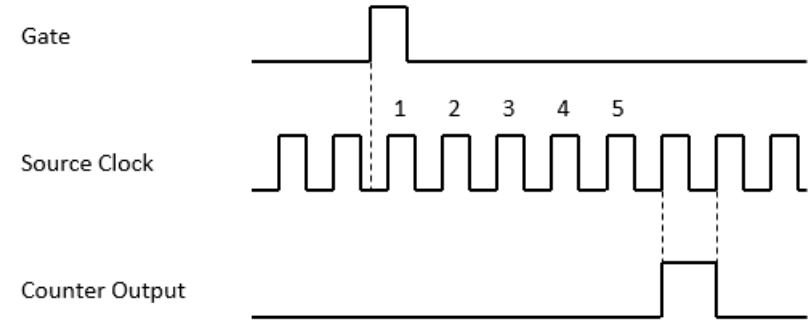

Figure 3.20 One-shot operation

3.5.5 Timer/Pulse

In timer/pulse mode, continuous pulses with specified frequency are generated at counter output terminal, and an interrupt is also generated with each pulse as shown in Figure 3. 21.

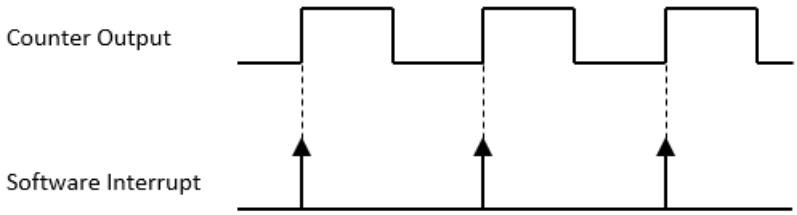

Figure 3.21 Pulse output and timer interrupt

The output can be gated. If counter gate is in active level, pulses are output normally. On the other hand, if counter gate is in inactive level, output is disabled. Figure 3. 22 shows an example of active high gate.

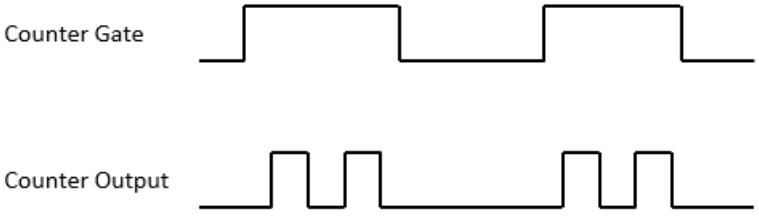

Figure 3.22 Gated timer/pulse output

Static (Software-Timed) Timer/Pulse

With static timer/pulse, the software controls the time of updating output pulse frequency, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the frequency of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3. 23.

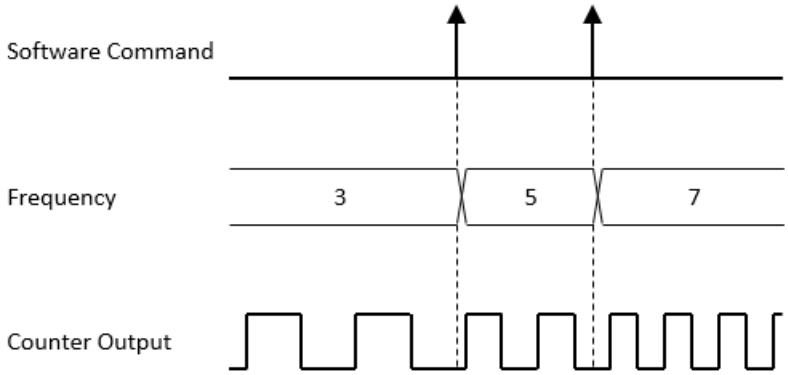

Figure 3.23 Static (software-timed) timer/pulse

3.5.6 Pulse Width Modulation Output

In pulse width modulation (PWM) output mode, a pulse waveform with specified high period (tHIGH) and low period (tLOW) is output at counter output terminal as shown in Figure 3. 24.

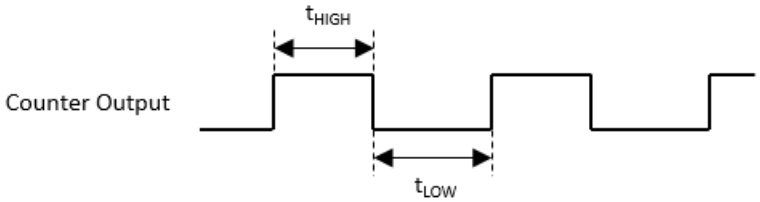

Figure 3.24 Pulse width modulation output

The number of pulses generated can be finite or infinite. For finite pulse generation, the counter output starts generating pulses when armed, and automatically stops after the specified number of pulses has completed. The counter can be re-armed after the previous generation is completed. This is shown in Figure 3. 25.

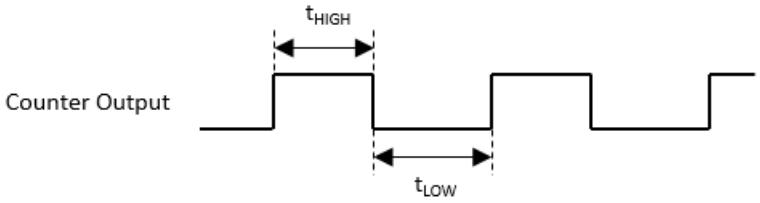

Figure 3.25 Finite pulse generation

For infinite pulse generation, the counter output starts generating pulses when armed and continues until stopped by software. This is shown in Figure 3. 26.

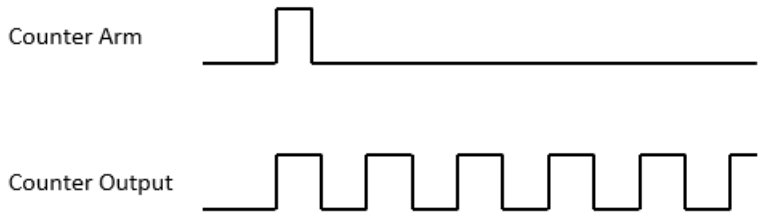

Figure 3.26 Infinite pulse generation

The output can be gated. If counter gate is high, pulses are output normally. On the other hand, if counter gate is low, output is disabled. This is shown in Figure 3. 27.

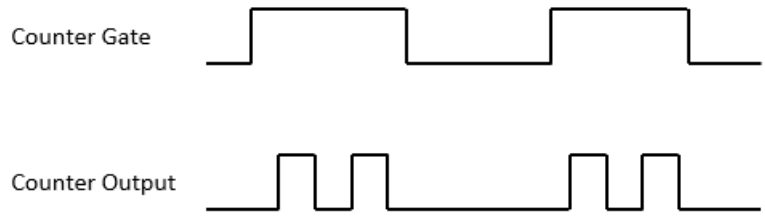

Figure 3.27 Gated pulse width modulation output

Static (Software-Timed) PWM Output

With static PWM output, the software controls the time of updating output pulse width, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the width of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3. 28.

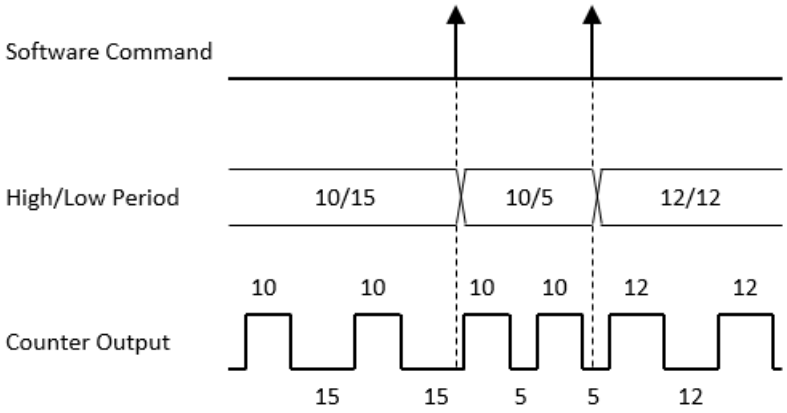

Figure 3.28 Static (software-timed) timer/pulse

3.6 Clock

The clock signal can be generated internally or provided from external source. For internal clock, when configuration is done, the clock frequency cannot be changed on the fly during the acquisition or generation operation. For external clock, on the other hand, clock frequency can be controlled by the external source in real time.

3.7 Synchronization

For the synchronization of multiple devices during acquisition, it is crucial to ensure the correct wiring of the necessary timing signals. All devices should utilize the same sample clock to maintain an equal sample rate and commence acquisition simultaneously through a start trigger. Designating one device as the master and others as slaves, the master device transmits the essential timing signals to synchronize acquisition across all slave devices.

The timing signals can be wired internally by the Multi-Device Synchronization Interface (MDSI) cables.

Synchronize by MDSI Cables

To use MDSI cable for synchronization, connect each cable between MDSI OUT of one device to MDSI IN of the next device as shown in Figure 3. 29.

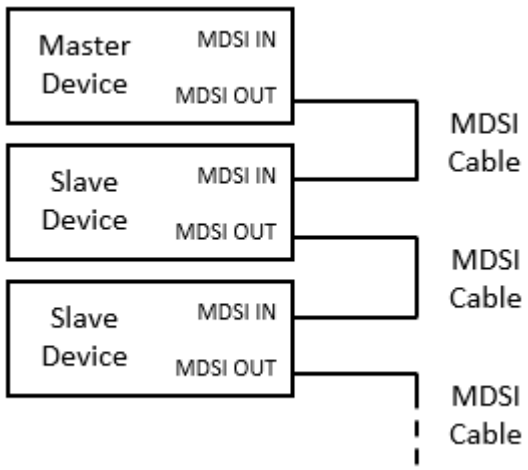

Figure 3.29 Synchronize multiple devices by MDSI cables

"Convert Clock Source" and "Trigger Source" configurations for the master can be selected as required. However, these configurations for the slaves must be selected according to Table 3. 1.

Table 3.1: Software configuration for synchronization using MDSI cable

Card	Master	Slave
Convert Clock Source	Internal Clock	External Digital Clock from MDSI pin
Trigger Source	None One of AI channels External Digital Trigger 0/1	MDSI Trigger 0/1

After all configurations are done, start all the slaves before the master. This ensures all the slaves are ready when the master sends synchronization signals.

3.8 Calibration

The Navigator of Advantech DAQNavi provides the calibration utility to calibrate the analog input and analog output circuitry of the device. Figure 3. 1 shows the interface of the calibration utility. Follow the instructions shown to calibrate the device. For a

multi-function device, which contains both analog input and analog output functions, analog input calibration must be performed before analog output calibration.

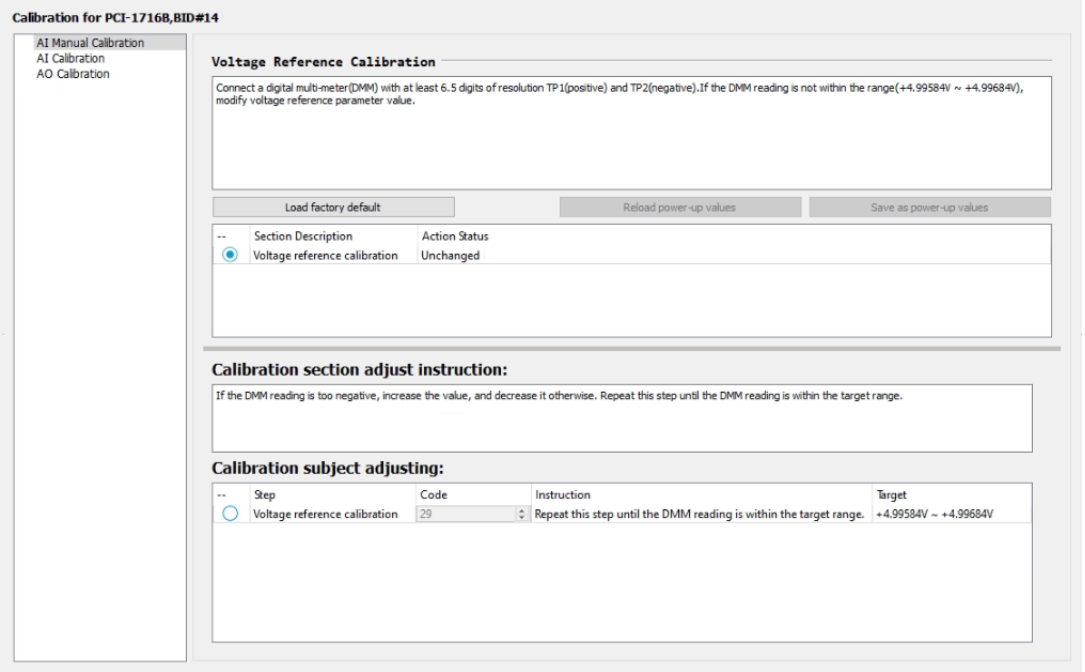

Figure 3.30 Calibration utility

Upon modifying any calibration parameter, users have the option to preserve the change by selecting the "Save as power-up values" button. Alternatively, they can reload power-up values by clicking the "Reload power-up values" button. The current status of the calibration parameters is displayed in the "Action Status" column. If necessary, users can restore the factory default calibration parameters by clicking the "Load factory default" button.

Appendix A

Specification

A.1 Function Block Diagram

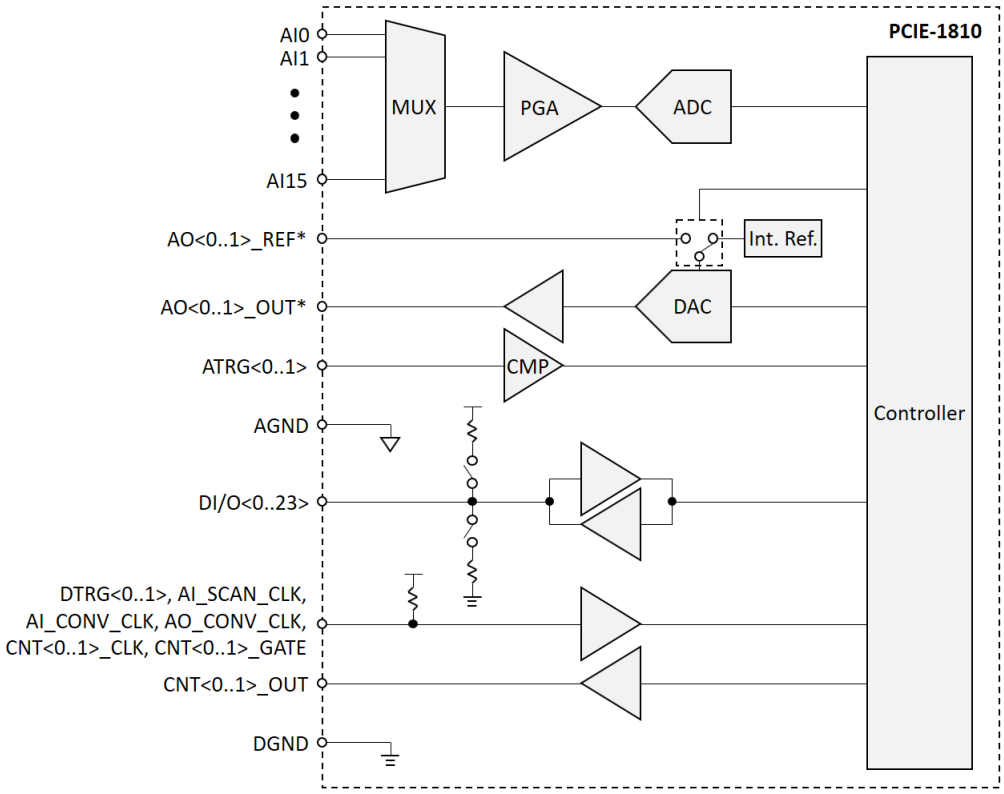

Figure A.1 Function Block

A.2 Analog Input

- **Channels:** 16 single-ended, 8 differential, or combination, software configurable
- **Analog-to-digital converter (ADC) resolution:** 12 bits
- **Input coupling:** DC
- **Input range:** ±10 V, ±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 ~ 10 V, 0 ~ 5 V, 0 ~ 2.5 V, or 0 ~ 1.25 V, software configurable per channel
- **Maximum input voltage:** ±11 V
- **Input common-mode voltage range:** ±11 V
- **Over-voltage protection:** ±15 V
- **Input impedance:** 1 GΩ

- **-3 dB bandwidth**

Table A.1: -3 dB Bandwidth

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
BW	4.5 MHz	4.2 MHz	4 MHz	2.9 MHz	2.2 MHz

- **Linearity**
  - **Integral non-linearity (INL):** ±1 LSB max.
  - **Differential non-linearity (DNL):** ±1 LSB max.

- **Absolute accuracy**

Operating temperature within ±5°C of last auto-calibration temperature

Table A.2: Accuracy

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
Accuracy	±0.1%	±0.1%	±0.2%	±0.2 %	±0.4%
Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
Accuracy		±0.1%	±0.2%	±0.2%	±0.4%

Over full operating temperature range

Table A.3: Accuracy

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
Accuracy	±0.5%	±0.5%	±1.0%	±1.0%	±2.0%
Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
Accuracy		±0.5%	±1.0%	±1.0%	±2.0%

- **Common-mode rejection ratio (CMRR):** 70 dB

DC performance

Table A.4: Idle Channel Noise

Range	50 kS/s		200 kS/s		500 kS/s	
	Noise **(μVRMS)**	Effective Resolution (bits)	Noise **(μVRMS)**	Effective Resolution (bits)	Noise **(μVRMS)**	Effective Resolution (bits)
±10 V	0	12	641	12	261	12
±5 V	69	12	10	12	719	12
±2.5 V	40	12	39	12	313	12
±1.25 V	13	12	114	12	103	12
±0.625 V	0	12	0	12	0	12
0 ~ 10 V	0	12	0	12	0	12
0 ~ 5 V	0	12	0	12	0	12
0 ~ 2.5 V	0	12	0	12	0	12
0 ~ 1.25 V	3	12	0	12	2	12

AC performance

Table A.5: Signal-to-Noise Ratio (SNR, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	50 kS/s	200 kS/s	500 kS/s	1 MS/s
±10 V	72.31	72.29	72.36	71.77
±5 V	72.35	71.43	72.14	72.17
±2.5 V	72.54	72.10	72.20	71.72
±1.25 V	70.43	70.69	71.25	70.51
±0.625 V	65.28	67.34	69.08	68.55

Table A.6: Total Harmonic Distortion (THD, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	50 kS/s	200 kS/s	500 kS/s	1 MS/s
±10 V	-85.15	-85.11	-87.33	-88.77
±5 V	-85.70	-84.88	-85.47	-91.37
±2.5 V	-88.33	-85.01	-86.54	-89.57
±1.25 V	-85.20	-85.53	-86.81	-87.52
±0.625 V	-82.96	-84.29	-86.51	-90.25

Table A.7: Total Harmonic Distortion Plus Noise (THD+N, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	50 kS/s	200 kS/s	500 kS/s	1 MS/s
±10 V	-72.09	-72.07	-72.22	-71.68
±5 V	-72.16	-71.23	-71.94	-72.12
±2.5 V	-72.43	-71.89	-72.05	-71.64
±1.25 V	-70.29	-70.55	-71.13	-70.43
±0.625 V	-65.20	-67.26	-69.01	-68.52

Table A.8: Spurious-Free Dynamic Range (SFDR, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	50 kS/s	200 kS/s	1 MS/s	500 kS/s
±10 V	88.06	84.32	84.68	79.01
±5 V	90.15	78.81	84.00	82.70
±2.5 V	87.32	85.49	84.51	81.90
±1.25 V	80.81	78.79	83.92	77.58
±0.625 V	71.29	72.76	75.11	72.77

Table A.9: Effective Number of Bits (ENOB, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**50 kS/s**	**200 kS/s**	**500 kS/s**	**1 MS/s**
±10 V	11.68	11.67	11.70	11.61
±5 V	11.69	11.54	11.65	11.68
±2.5 V	11.73	11.64	11.67	11.60
±1.25 V	11.38	11.42	11.52	11.40
±0.625 V	10.53	10.88	11.17	11.09

Table A.10: Signal to Noise and Distortion (SINAD, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**50 kS/s**	**200 kS/s**	**500 kS/s**	**1 MS/s**
±10 V	72.09	72.07	72.22	71.68
±5 V	72.16	71.23	74.94	72.12
±2.5 V	72.43	71.89	72.05	71.64
±1.25 V	70.29	70.55	71.13	70.43
±0.625 V	65.20	67.26	69.01	68.52

- **Acquisition type:** Instant or buffered, software configurable
- **Buffered acquisition**
  - **Enable channel combination:** Each channel can be enabled/disabled independently by software
  - **Scan clock source:** Internal or external
- **Convert clock rate**
  - **Single channel:** 1 MHz max., software configurable (Internal clock) 500 KHz max., software configurable (External clock)
  - **Multi-channel:** 1 MHz shared by all enabled channels, software configurable
- **Convert clock source:** Internal or external
- **Internal data buffer (FIFO) size:** 8,192 samples

A.3 Analog Output

- **Channels:** 2
- **Digital-to-analog converter (DAC) resolution:** 12 bits
- **Output configuration:** Single-ended
- **Output coupling:** DC
- **Output range**
  - **Reference source:** Internal or external, software configurable per channel
  - **Internal reference:** ±10 V, ±5 V, 0 ~ 10 V, or 0 ~ 5 V, software configurable per channel
  - **External reference:** ±x V or 0 ~ +x V @ +x V reference (-10 ≤ x ≤ +10), software configurable per channel
- **Power-on state:** 0 V @ ±10 V output range
- **Driving capability:**±20 mA max.
- **Output impedance:**0.1 Ω max.
- **Linearity**
  - **Integral non-linearity (INL):** ±1 LSB max.
  - **Differential non-linearity (DNL):** ±1 LSB max.
- **Absolute accuracy**
  - **Operating temperature within ±5°C of last auto-calibration temperature:** ±0.1% of full-scale range max.
  - **Over full operating temperature range:** ±0.5% of full-scale range max.
- **Power-on glitch:** 50 mV
- **DC performance**
  - **Output noise:** 0.5 mV
  - **Effective resolution:** 12 bits
- **Channel-to-channel DC crosstalk:** -140 dB
- **AC performance**
  - **Slew rate:** 20 V/μs
  - **Settling time:** 15 μs (to 1% of FSR)
- **Update type:** Static or buffered, software configurable
- **Buffered generation**
  - **Enable channel combination:** Each channel can be enabled/disabled independently by software
  - **Update clock rate:** 500 kHz max. per channel, software configurable
  - **Update clock source:** Internal or external
  - **Internal data buffer (FIFO) size:** 8,192 samples

A.4 Bi-directional Digital Input/Output

- **Channels:** 24
- **Direction control:** Each nibble can be configured independently by software, or can be fixed as output by on-board jumpers
- **Power-on state:** Input when controlled by software, output when set by jumpers

A.4.1 Digital Input

- **Input type:** 5 V TTL
- **Input logic level**
  - **Logic high:** 2.0 V min.
  - **Logic low:** 0.8 V max.
  - **Working voltage:** -0.25 V ~ 5.25 V
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 10 kΩ (default) or pull-down 10 kΩ, software configurable
- **Response time:** 25 ns max.
- **Debounce filter:** 32 ns ~ 67 ms, software configurable
- **Acquisition type:** Instant or buffered, software configurable
- **Buffered acquisition:**
  - **Enabled channel combination:** Each port can be enabled/disabled independently by software
  - **Sample clock rate:** 1 MHz max. per channel, software configurable
  - **Sample clock source:** Internal or external
  - **Internal data buffer (FIFO) size:** 4,096 samples
- **Interrupt**
  - **Edge detection:** Rising edge, falling edge, or both edges, software configurable per channel
  - **Pattern match detection:** By port detection, each channel can be enabled or disabled by software independently
  - **State latch:** Latch port state when interrupt occurs

A.4.2 Digital Output

- **Output type:** 5 V TTL
- **Power-on state:** Logic low
- **Output logic level**
  - **Logic high:** 4.0 V min. @ 2 mA source/5.2 V max.
  - **Logic low:** 0.4 V max. @ 2 mA sink
- **Load current**
  - **One channel:** 8 mA max.
  - **Per port summed:** 20 mA max.
  - **Response time:** 25 ns max.
  - **Update type:** Static or buffered, software configurable
- **Buffered generation**
  - **Enabled channel combination:** Each port can be enabled/disabled independently by software
  - **Update clock rate:** 1 MHz max. per channel, software configurable
  - **Update clock source:** Internal or external
  - **Internal data buffer (FIFO) size:** 4,096 samples
- **Initial output value:** Configurable by software

A.5 Trigger

- **Number of triggers:** 2
- **Trigger action:** Start, delay to start, stop, or delay to stop
- **Trigger delay range:** 0 ~ 16,777,215 samples
- **Sample number:** 0 ~ 16,777,215 samples
- **Analog trigger**
  - **Source:** 2 external pin
  - **Input range:** ±10 V
    - ► **Resolution:** 16 bits
    - ► **Accuracy:** ±0.5% of full-scale range max.
    - ► **Polarity:** Rising edge or falling edge, software configurable
    - ► **Input protection voltage:** ±15 V
    - ► **Minimum width:** 100 ns
- **Digital trigger**
  - **Source:** 2 external pins
  - **Input logic level**
    - ►**Logic high:** 2.0 V min.
    - ►**Logic low:** 0.8 V min.
    - ►**Working voltage:** -0.25 V ~ 5.25 V
    - ►**Polarity:** Rising edge or falling edge, software configurable
    - ►**Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 10 kΩ
- **Minimum width:** 100 ns

A.6 External Clock Input

- **Channels:** 2 conversion clocks/1 scan clock
- **Input type:** 5 V TTL
- **Input logic level:**
  - **Logic high:** 2.0 V min.
  - **Logic low:** 0.8 V max.
  - **Working voltage:** -0.25 V ~ 5.25 V
- **Polarity:** Rising edge
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 10 kΩ
- **Minimum width:** 100 ns

A.7 Multi-Device Synchronization Interface (MDSI)

- **Multi-device synchronization interface (MDSI):** Yes, connected by 10-pin flat cable

A.8 Counter

- **Channels:** 2
- **Resolution:** 32 bits
- **Input type:** 5 V TTL
- **Input logic level:**
  - **Logic high:** 2.0 V min.
  - **Logic low:** 0.8 V max.
  - **Working voltage:** -0.25 V ~ 5.25 V
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 10 kΩ
- **Debounce filter:** 32 ns ~ 67 ms, software configurable
- **Output type:** 5 V TTL
- **Output logic level:**
  - **Logic high:** 4.0 V min. @ 2 mA source/5.2 V max.
  - **Logic low:** 0.4 V max. @ 2 mA sink
- **Load current:** 8 mA max.
- **Counter measurement function**
- **Event counting**
  - **Input frequency:** 10 MHz max.
  - **Clock polarity:** Rising edge or falling edge, software configurable
  - **Gate function:** Enabled or disabled, software configurable
  - **Gate polarity:** High active or low active, software configurable
  - **Measuring type:** Instant
- **Frequency measurement**
  - **Measuring method:** Counting pulse by system time, period inverse, or auto adaptive, software configurable
  - **Input frequency:** 0.1 Hz ~ 10 MHz
  - **Accuracy:** fIN/40 MHz or 50 ppm, whichever is larger
  - **Measuring type:** Instant
- **Pulse width measurement**
  - **Pulse width range:** 100 ns ~ 1 s
  - **Pulse width resolution:** 25 ns
  - **Accuracy:** 50 ppm
  - **Measuring type:** Instant
- **Counter output function**
- **One shot**
  - **Internal clock source frequency:** 10 MHz, 1 MHz, 100 kHz, or 10 kHz, software configurable
  - **Internal clock accuracy:** 50 ppm
  - **External clock source frequency:** 10 MHz max.
  - **Delay count:** 1 ~ 4,294,967,295
  - **Gate source:** External
  - **Gate polarity:** Rising edge or falling edge, software configurable
  - **Output signal type:** Positive pulse or negative pulse, software configurable
  - **Generation type:** Static
- **Timer/pulse**
  - **Timebase clock frequency:** 40 MHz
  - **Timebase clock accuracy:** 50 ppm

- **Output frequency:** 0.1 Hz ~ 10 MHz
- **Gate function:** Enabled or disabled, software configurable
- **Gate polarity:** High active or low active, software configurable
- **Interrupt generation:** Enabled or disabled, software configurable
- **Generation type:** Static

- **Pulse width modulation**
  - **Timebase clock frequency:** 40 MHz
  - **Timebase clock accuracy:** 50 ppm
  - **Pulse width:** 100 ns ~ 1 s
  - **Pulse width resolution:** 25 ns
  - **Number of pulses:** 1 ~ 4,294,967,295 or infinite, software configurable
  - **Gate function:** Enabled or disabled, software configurable
  - **Gate polarity:** High active or low active, software configurable
  - **Generation type:** Static

A.9 FPGA Code Update

FPGA code update function: Yes, through Advantech Navigator utility

A.10 General Specifications

A.10.1 Power Requirements

- **Power consumption**
  - **+3.3 V:** 350 mA max.
  - **+12 V:** 250 mA max.

A.10.2 Power Supply Output

- **+5 V (±5%):** 200 mA max.
- **+12 V (±5%):** 100 mA max.

A.10.3 Physical

- **Form factor:** PCIe x1
- **Dimensions:** 175 x 100 x 18 mm3 (6.9 x 3.9 x 0.7 in.3)
- **Weight:** 115 g
- **I/O connector:** 68-pin SCSI (pin type)

A.10.4 Environmental

- **Operating temperature:** 0 °C to 60 °C (32 °F to 140 °F)
- **Storage temperature:** -20 °C to 70 °C (-4 °F to 158 °F)
- **Operating humidity:** 10% to 90% RH, non-condensing
- **Storage humidity:** 5% to 95% RH, non-condensing

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