

User Manual

MIC-3328

3U CompactPCI Intel Ivy bridge Dual/Quad Core Processor Blade



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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

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Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Warnings, Cautions and Notes



Warning! Warnings indicate conditions, which if not observed, can cause personal injury!





Caution! Cautions are included to help you avoid damaging hardware or losing data. e.g. There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.



Notes provide optional additional information.

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- MIC-3328 single board computer (CPU and PCH heatsink included) x1
- Daughter board for SATA HDD, HDD tray (Assembled with SBC dual slot 8HP-1 version) x 1
- Warranty certificate document x 1
- M2.5*8L screw x1 and plastic SPACER SUPPORT x1 in accessory bag for CFast fixing when you plugged in a CFast card
- M3*5L screw x4 in accessory bag for HDD/SSD fixing when you installed HDD/ SSD
- 2PIN Jumper in accessory bag for CMOS Clear

Safety Instructions

- 1. Read these safety instructions carefully.
- 2. Keep this User Manual for later reference.
- 3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
- 4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
- 5. Keep this equipment away from humidity.
- 6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
- 7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
- 8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
- 9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
- 10. All cautions and warnings on the equipment should be noted.
- 11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
- 12. Never pour any liquid into an opening. This may cause fire or electrical shock.
- 13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
- 14. If one of the following situations arises, get the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated into the equipment.
 - The equipment has been exposed to moisture.
 - The equipment does not work well, or you cannot get it to work according to the user's manual.
 - The equipment has been dropped and damaged.
 - The equipment has obvious signs of breakage.
- 15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
- 16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

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MIC-3328 User Manual



Hardware Configuration

This chapter describes how to configure MIC-3328 hardware.

1.1 Introduction

Advantech's MIC-3328 is a 3U CompactPCI PlusIO CPU blade based on the Intel® 3rd generation Core[™] processor family. Based on latest 22 nm process technology these processors support up to four cores / eight threads at up to 2.5 GHz and up to 6M last level cache. With Intel HD Graphics (Gen7, DX11, OCL1.1) integrated into the CPU, the MIC-3328 can serve applications demanding high performance, high resolution video output on up to three independent display interfaces. Latest DDR3 DRAM up to 8 GB running at 1600MT/s complement the powerful processor with high performance, ECC protected onboard memory.

MIC-3328's design for reliability like using soldered processor, DRAM and flash storage for enhanced shock and vibration tolerance make it an ideal choice for workstation workloads in harsh environments and mission/business-critical applications such as military, transportation, test & measurement and traffic control. The enhanced fixed point and floating point performance offered by the intel CoreTM processor, improvements in the vector processing instruction set (AVX) along with the possibility to utilize the integrated GPU via standard interfaces such as OpenCL make the MIC-3328 also a great fit for signal processing applications such as radar, beam forming or image processing.

For best in class IO performance, MIC-3328 uses the Intel QM77 PCH, which provides extensive I/O support such as USB3.0, PCI Express gen.2 and SATA-III ports.

For dense applications the MIC-3328 is available with a 4HP front panel, occupying a single slot, only. For applications requiring additional IO and/or peripheral support, the MIC-3328 can be extended to 8HP (2 slots) via specific extension modules (XTMs). For industrial display or workstation applications, a graphics-centric XTM routes two Display Ports from the PCH for triple display support, adds 2 COM ports for data acquisition and control plus a PS/2 and 2.5" SSD. A second XTM provides a XMC mezzanine slot for industry standard extension modules like Advantech's MIC-3666 dual 10GE adapter card. The XMC slot supports a PCI Express x8 interface directly into the Intel CoreTM processor with speeds up to 64Gbps according to PCI Express 3.0.

While support for legacy CompactPCI is provided on J1 via an onboard PI7C9X110 bridge, the MIC-3328 supports an UHM J2 connector according to PCIMG2.30 (PlusIO). While this connector maintains backwards compatibility and interoperability with legacy systems, it makes state of the art serial interfaces such as Gigabit Ethernet, PCI express, USB and SATA available for use on a Rear transition Module (RTM) or on a hybrid backplane supporting legacy IO cards as well as CompactPCI Serial peripheral cards as defined in PICMG2.30. Thus, MIC-3328 provides a smooth, risk free and future proof migration path from legacy parallel PCI bussed CompactPCI system to latest serial interface standard predominant in the computer industry. With full backwards compatibility to CompactPCI, customers investments stay protected while the door is opened for platform enhancements and innovations via the new serial interfaces. The MIC-3328 PlusIO J2 supports interfaces such as 4 PCI Express x1 gen. 2 links for IO extension, one GbE for computer to computer multiprocessing, three SATA for Hard drives and RAID systems as well as 4 USB ports for wireless interfaces and legacy interface replacement.

Table 1.1: MIC-3328 Variants									
Model number	MIC-3328X [*] 1-S1E	MIC-3328X [*] 1-D1E	MIC-3328X [*] 1-D2E						
Slot Width	Single Slot (4HP)	Dual Slots (8HP-1)	Dual Slots (8HP-2)						
2 nd Layer XTM	-	1	1						
Storage	Optional NAND Flash	CFast/SATA SSD	CFast/ Optional NAND Flash						

 $X^* = A/B/C$

- A mean CPU is 3517UE,17W
- B mean CPU is 3555LE, 25W
- C mean CPU is 3612QE, 35W

1.2 Specifications

1.2.1 CompactPCI Bus Interface

Table 4.0. ODU Varia

The MIC-3328 is compliant with PICMG 2.0 Rev. 3.0 and PICMG 3.0 CPCI PlusIO specification. It supports a 32-bit / 33 MHz PCI bus for up to 8 CompactPCI slots at 3.3 V or 5 V VIO. The MIC-3328 is hot-swap compliant (PICMG 2.1).

1.2.2 CPU

The MIC-3328 supports the 22nm technology Intel® IvyBridge[™] 3612QE / 355LE / 3517UE processors with clock frequencies up to 2.5GHz and DMI 5GB/s. Supported processors are listed in the table below. The forced airflow cooling is required.

Intel CPU Model	Cores	Freq.	Package	Cache	CPU TDP	Board Power Consumption	Required Airflow		
3517UE(8HP)	2	1.7 GHz	BGA	4MB	17 W	23.42 W	5CFM		
3555LE(8HP)	2	2.5 GHz	BGA	4MB	25 W	33.12 W	10CFM		
3612QE(8HP)	4	2.1 GHz	BGA	6MB	35 W	43.91 W	20CFM		

1.2.3 **BIOS**

A 8-MByte SPI flash contain a board-specific UEFI BIOS (from AMI) designed to meet industrial and embedded system requirements.

1.2.4 Chipset

MIC-3328 uses the Intel QM77 PCH, which provides extensive I/O support such as USB3.0, PCI Express gen.2 and SATA-III ports. Three i210 Gigabit Ethernet Controllers provide front panel as well as rear panel network connectivity.

Table 1.3:	MIC	-3328	with 8H	IP-1 I	/O Fea	atur	es				
	Fron	Front Panel-4HP			Front Panel-8HP			Main On-Board Features			
System Board	VGA	USB3.0	Ethernet (RJ45)	СОМ * ①	Display port	' PS/2	Onboard Memory	CFast	SATA SSD	СОМ* ②	on board SATA flash
											Mini-PCle
MIC-3328A1- D1E	1	2	2	2	2	1	4GB	1	1	2	optional
MIC-3328B1- D1E	1	2	2	2	2	1	8GB	1	1	2	optional
MIC-3328C1- D1E	1	2	2	2	2	1	8GB	1	1	2	optional

Note!

COM* (1), RJ45 COM with RS232.



COM* ② ,PIN Header with RS232/422/485,these COM PIN Headers, SATA SSD and XMC are mutually exclusive.

Table 1.4: MIC-3328 with 8HP-2 I/O Features										
	Front	Panel-4H	Р	Front	Panel-8HP	Main On-Boa	ard Features			
System Board	VGA	USB3.0	Ethernet (RJ45)	ХМС	USB2.0* (type A)	Onboard CPU	Onboard Memory	CFast		
MIC-3328A1-D2E	1	2	2	1	2	I7-3517UE	4GB	1		
MIC-3328B1-D2E	1	2	2	1	2	17-3555LE	8GB	1		
MIC-3328C1-D2E	1	2	2	1	2	17-3612QE	8GB	1		

1.2.5 Memory

The MIC-3328 has 4GB of on-board DDR3-1600 SDRAM on 17W 3517UE version. The MIC-3328 has 8GB of on-board DDR3-1600 SDRAM on 25W 3555LE and 35 W 3612QE version.

1.2.6 Ethernet

There are three I/O LAN ports on the MIC-3328, which are implemented using three Intel i210AT LAN controllers to provide 10/100/1000 Base-T Ethernet connectivity. Three i210 Gigabit Ethernet Controllers provide front panel as well as rear panel network connectivity. The i210 provides higher performance over previous Gigabit Ethernet controllers, better support for virtualization, Energy Efficient Ethernet and ECC protected packet buffers for enhanced reliability. Support for time stamping and synchronization is accomplished via IEEE1588 (PTP). Support for industrial Ethernet protocols such as ProfiNet, EtherCAT and Powerlink is available via third party software partners.

1.2.7 Storage Interface

The MIC-3328 supports three SATA channels. Three SATA on front 4HP and 8HP.Three SATA interfaces are routed to the RIO via the J2 3M UHM connector for PlusIO application.

Table 1.5: Storage									
Storage	on board SATA NAND Flash	CFast	SATA SSD/HDD	3 SATA					
Location	4HP	8HP-1	8HP-1	to J2					

1.2.8 Serial Interface

Four UARTs (serial ports) are on the second layer, and 2 RS232 ports to 8HP front ,2 RS232/422/485 ports are on board PIN header or to 8HP RIO.

1.2.9 USB Port

Two USB3.0 and Six USB 2.0 compliant ports are provided. Two USB3.0 ports are routed to front panel connectors; Two USB2.0 routed to second layer (could be designed on 8HP-2 front panel). The other four USB2.0 ports are routed to J2 UHM connector for PlusIO application.

1.2.10 LEDs

Three LEDs are provided on the front panel as follows:

Table 1.6: LED Indicator for the MIC-3328							
LED	Color	Indicator					
Hot swap	Blue	The board could be safely removed					
Power	Green	Power is provided to the board					
חחח	Green	HDD power is on					
	Blinking	HDD is accessed					

1.2.11 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control. The programmable time interval is from 1 to 255 seconds.

1.2.12 Optional Rear I/O Modules

The MIC-3526R1-S1E is the optional 4HP RTM (also known as rear I/O module) for the MIC-3328. It offers a wide variety of I/O panel features, such as one RJ45 LAN ports, and four USB2.0 ports. It also comes with on-board features such as three SATA (one SATA socket for mSATA, two SATA PIN header) and one miniPCIe (for wireless LAN card).

Table 1.7: RIO Configurations								
RTM Model Number	Rear Panel 4HP		Rear Panel 8HP		All Onboard Socket are on 4HP			
	USB	LAN	DP	COM*	PS/2	SATA	PCle	Slot
MIC-3526R1-D1E	4	1	2	2	1	3	1	2
MIC-3526R1-S1E	4	1	-	-	-	3	1	1

- Note!
- 1. PS/2 is mutually exclusive with PS/2 on 8HP front panel by BOM control. It required a special 8HP board to work. The special 8HP board is on request by customer.
- 2. 2 x COM default setting is RS232, RS422/485 could be set by the switch on 8HP board. (Total 4 COM ports on 8HP and it's RIO)
- 3. 2 x DisplayPort is switchable from front panel by switch on 8HP board.

1.2.13 Optional Extension Modules

The MIC-3328 has two kinds of second layer XTM. One XTM 8HP-1 is used for multidisplay dual-slot platform, and rich I/O feature set such as COM, PS/2, SATA SSD...etc. Another XTM 8HP-2 is used for XMC PCIe x8 based dual-slot platform. The XTM pin assignment and connectivity is described in detail in the Appendix. For a customized extension module demand, please contact Advantech local representative.

Table 1.8: The Second Layer XTM (8HP) Configurations								
хтм	IO Panel			On-board Header/Socket/ Connector				
	Display port	COM * (1) PS/2	USB	ХМС	SATA HDD	Cfast	COM* 2
8HP-1	2	2	2	-	-	1	1	2
8HP-2	-	-	-	2-optional	1	-	1	2

Note!

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COM* ①: RJ45 COM with RS232.

COM* ② : PIN Header with RS232/422/485(switchable to RIO),these COM PIN Headers, SATA SSD and XMC are mutually exclusive.

1.2.14 Mechanical and Environmental Specifications

Operating temperature: 0 ~ 60°C (32 ~ 140°F)

The operating temperature range of the MIC-3328 depends on the installed processor and the airflow through the chassis. Detail airflow information please refer to Table1.2.For extended temperature products please contact your ADVANTECH representative.

- Storage Temperature: -40 ~ 85°C (-40 ~ 185°F)
- Humidity (operating): 95% @ 60°C (non-condensing)
- Humidity (Non-operating): 95% @ 60°C (non-condensing)
- Vibration (Random operating): 5 ~ 500 Hz, 2 Grms (without on-board 2.5"HDD)
- Vibration (Sine Non-operating): 5 ~ 500 Hz, 2 Grms (without on-board 2.5" HDD)
- Shock (operating): 10 G each face operating three times
- Shock (Non-operating):30 G each face Non-operating three times
- Board size:
 - 3U/1 slot width (4HP): 100 x 160 x 20 mm (3.9" x 6.3" x 0.8")
 - 3U/2 slot width (8HP): 100 x 160 x 40 mm (3.9" x 6.3" x 1.6")
- Net Weight:
 - 3U/1 slot width (4HP): 0.62 kg
 - 3U/2 slot width (8HP): 0.90 kg

1.2.15 Compact Mechanical Design

MIC-3328 series has a specially designed heat sink for the processor. MIC-3328 17w and 25w series is installed with aluminum heatsink, MIC-3328 35w series is installed with cuprum heatsink. However, forced air cooling in the chassis is still needed for operational stability and reliability to MIC-3328 all series.

1.2.16 CompactPCI Bridge

The MIC-3328 uses a Pericom PCIe to PCI bridge as a gateway to an intelligent subsystem. The PI7C9X110 bridge offers the following features:

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1
- Compliant with PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a
- PME support
- 3.3 V PCI signaling with 5V I/O tolerance
- Provides two level arbitration support for eight PCI Bus masters
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support

Note!

PCI INT interrupt or MSI Function support

Please consult the PI7C9X110 data sheet for more details.

1.2.17 Hardware Monitor

One Hardware Monitor (NCT7904D) is available to monitor critical hardware parameters, such as system temperature and core voltage.

1.2.18 Super I/O

The MIC-3328 Super I/O (SCH3106) device provides the following legacy PC devices:

- Two UART ports are connected to the XTM as RS232 COM1 and COM2 on front panel. Two UART ports are connected to RIO via J2 as two on board RS-232/422/485
- The PS2 (keyboard/mouse) is routed to the XTM as PS/2 IO on the front panel.

1.2.19 RTC and Battery

The RTC module keeps the date and time. On the MIC-3328 model the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3 V, 210 mAh).

1.2.20 Drone Mode

The Drone mode will be automatically implemented when the CPU blade is plugged in the peripheral slot on the backplane.

1.3 Functional Block Diagram



1.4 Jumpers and Switches

Table 1.9 and Table 1.10 list the jumper and switch functions. Figure 1.2 illustrates the jumper and switch locations.

The MIC-3328 provides a system reset button (RST near to USB connector) located on the front panel. The system reset button resets all payload and application-related circuitry.

Please read this section carefully before changing the jumper and switch settings on MIC-3328.



You should use a two PIN jumper to short the CN2 PIN1 and PIN2 when you want clear CMOS.

1 2 3

Table 1.9: MIC-3328 jumper descriptions					
Number	Function	PIN NO.	PIN Definition		
CN2	for Clear CMOS	PIN1	RTCRST		
CN2	for Clear CMOS	PIN2	GND		
CN5	for CPLD programming	PIN1	PWR		
CN5	for CPLD programming	PIN2	TDO		
CN5	for CPLD programming	PIN3	TDI		
CN5	for CPLD programming	PIN4	EN		
CN5	for CPLD programming	PIN5	N/A		
CN5	for CPLD programming	PIN6	TMS		
CN5	for CPLD programming	PIN7	GND		
CN5	for CPLD programming	PIN8	ТСК		



Figure 1.2 MIC-3328 jumper locations

Table 1.10: MIC-3328 8HP Jumper Descriptions		
Number	Function	
SW1,SW2	For on board/8HP RIO COM3 setting	
SW3,SW4	For on board/8HP RIO COM4 setting	

SW5,SW6,SW7 For display setting

SW1 & SW2: (For on board/8HP RIO COM3 setting)



Figure 1.3 MIC-3328 COM3 switch setting

SW3 & SW4: (For on board/8HP RIO COM4 setting)

	COM setting	g ∎:key
	SW3	SW4
RS232 (Default)	1 2 3 4 5 6	1 2 3 4 5 6
	SW3	SW4
RS422	1 2 3 4 5 6	1 2 3 4 5 6
	SW3	SW4
RS485	1 2 3 4 5 6	1 2 3 4 5 6



SW5 & SW6 & SW7: (For Display Port setting)



Figure 1.5 MIC-3328 8HP Display Port switch setting



Figure 1.6 MIC-3328 switch locations

1.5 Connector Definitions

Table 1.11 lists the function of each connector and Figure 1.3 and 1.4 illustrate each connector location.

Table 1.11:	MIC-3328 4HP Connector Descriptions
Number	Function
USB3CN1	USB3.0 connector
USB3CN2	USB3.0 connector
CN3	Battery connector
CN4	XTM connector (8HP)
CN6	VGA(DB-15)
CN7	RJ45 LAN existing
CN8	XTM connector (8HP)
CN9	XTM connector (8HP)
CN10	Handle connecting
J1	Primary CompactPCI bus
J2	PlusIO or Rear I/O transition

Number Function CN1 USB connector	
CN1 USB connector	
CN2 USB connector	
CN3 RJ45 COM connector	
CN4 Cfast connector	
CN5 display port connector	
CN6 COM port pin header	
CN7 SATA Flash connector	
CN8 display port connector	
CN9 COM port pin header	
CN10 KB/MS connector	
CN11 MINIPCIEXPRESS LATCH	
CN12 MINIPCIEXPRESS connector	
CN15 Enable/disable radio operation on add-in cards that implement radio f quency applications	re-
CN16 USB connector	
CN17 HD Audio connector	
CN18 XTM connector (4HP)	
CN19 XTM connector (4HP)	
CN20 XTM connector (4HP)	
CN21 XTM connector (4HP)	
CN22 MPCIE LED connector	
XMC XMC connector	



Figure 1.7 MIC-3328 8HP-1 Front Panel Ports, Indicators and Buttons



Figure 1.8 MIC-3328 8HP-2 Front Panel Ports, Indicators and Buttons



Figure 1.9 MIC-3328 8HP-1 side view



Figure 1.10 MIC-3328 8HP-2 side view









Figure 1.13 RIO 8HP side view

Table 1.13: MIC-3328 4HP Rear I/O Connector Descriptions				
Number	Function			
CN1	MiniSATA connector			
CN2	SATA connector			
CN3	RJ45 LAN connector			
CN4	USB connector			
CN5	SATA connector			
CN6	USB connector			
CN7	MiniSATA Latch			
CN8	USB connector			
CN9	enable/disable radio operation on add-in cards that implement radio frequency applications			
CN10	Mini PCIE slot			
CN11	Mini PCIE Latch			
CN12	USB connector			
CN22	Mini PCIE LED connector			

Table 1.14: MIC-3328 8HP Rear I/O Connector Descriptions

Number	Function
CN1	KB/MS connector
CN2	RJ45 COM connector
CN3	RJ45 COM connector
CN4	Display port connector
CN5	Display port connector

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your CompactPCI chassis before you work on it. Don't touch any components on the CPU board or other boards while the CompactPCI chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installation Steps

The MIC-3328 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an anti-static workbench.

1.7.1 MIC-3328 Installation Steps



Figure 1.14 MIC-3328 8HP-1 assembly



Figure 1.15 MIC-3328 8HP-2 assembly



! The Screw and space support part was in accessory bag.

1.7.2 MIC-3328 Rear I/O Board Installation Steps

The MIC-3328 supports either rear I/O board. Following picture shows the installation of the rear I/O board.



Figure 1.16 MIC-3526 RIO for MIC-3328 8HP assembly

1.7.3 MIC-3328 Board Installation in PlusIO System

The MIC-3328 supports as PlusIO system mother board. Following picture shows the installation.



Figure 1.17 MIC-3328 Application in PlusIO system

1.8 Battery Replacement

The Battery model number is CR2032M1S8-LF, a 3V, 210 mAh battery. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact with your local Sales to check the availability.

PN: 1750129010 - BATTERY 3V/210 mAh with WIRE ASS'Y CR2032M1S8-LF

Batteries, battery packs, and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.

1.9 Software Support

Windows XP(Limited to IDE mode set under BIOS SATA Configuration,AHCI mode is not supported under Windows XP.), Windows 7, Windows 8, Windows server2008,Vxworks,UEFI OS and Red Hat Enterprise Linux 6.1 have been fully tested on the MIC-3328. Please contact your local sales representative for details on support for other operating systems.



AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for over a decade. This section describes the BIOS which has been specifically adapted to the MIC-3328. With the AMI UEFI BIOS Setup Utility, you can modify BIOS settings and control the special features of the MIC-3328. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-3328 setup screens.

Aptio Setup Utility Main Advanced Chipset Boot Se	– Copyright (C) 2012 America curity Save & Exit	n Megatrends, Inc.
BIOS Vendor Core Version Compliancy BIOS Information Build Date and Time CPLD Version	American Megatrends 4.6.5.4 UEFI 2.3.1; PI 1.2 MIC-3328V036 03/05/2014 14:15:16 0109	Set the Date. Use Tab to switch between Date elements.
IGFX VBIOS Version Memory RC Version Total Memory Memory Frequency	2158 1.8.0.0 8192 MB (DDR3) 1600 Mhz	
PCH Information Name Stepping TXT Capability of Platform/PCH	PantherPoint 04/C1 Supported	++: Select Screen 14: Select Item Enter: Select +(-: Change Ont
ME FW Version ME Firmware SKU	8.0.20.1513 5MB	F1: General Help F2: Previous Values F3: Optimized Defaults
System Date System Time	[Fri 01/02/2009] [00:27:23]	F4: Save & Exit ESC: Exit
Access Level	Administrator	
Version 2.15.1236.	Copyright (C) 2012 American	Megatrends, Inc.

Figure 2.1 Setup program initial screen

The BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed up CMOS so it retains the Setup information when the power is turned off.

2.2 Entering Setup

Turn on the computer, and there should be a POST (Power-On Self Test) screen that shows the BIOS supporting the CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that the CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press and you will immediately be allowed to enter Setup.



Figure 2.2 Press or <F2> to run setup

2.2.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

Aptio Setup Utili Main Advanced Chipset Boot	ty – Copyright (C) 2012 America Security Save & Exit	n Megatrends, Inc.
BIOS Vendor Core Version Compliancy BIOS Information Build Date and Time CPLD Version	American Megatrends 4.6.5.4 UEFI 2.3.1; PI 1.2 MIC-3328V036 03/05/2014 14:15:16 0109	Set the Date. Use Tab to switch between Date elements.
IGFX VBIOS Version Memory RC Version Total Memory Memory Frequency	2158 1.8.0.0 8192 MB (DDR3) 1600 Mhz	
PCH Information	PantherPoint	++: Select Screen
Stepping	04/C1	14: Select Item
TXT Capability of Platform/PCH	Supported	Enter: Select
ME EW Vencion	9 0 20 1512	+/-: Change Upt.
ME Firmware SKU	5MB	F2: Previous Values F3: Optimized Defaults
System Date	[Fri 01/02/2009]	F4: Save & Exit
System Time	[00:27:23]	ESC: Exit
Access Level	Administrator	
Version 2.15.123	6. Copyright (C) 2012 American	Megatrends, Inc.

Figure 2.3 Main setup screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured while options in blue can. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Chapter 2 AMI BIOS Setup

2.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIC-3328 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.



Figure 2.4 Advanced BIOS features setup screen

2.2.2.1 Trusted Computing



Figure 2.5 Trusted Computing

This item allows you to enable or disable Security Device Support; the default setting is "Disable".

2.2.2.2 CPU Configuration

Aptio Setup Utility Advanced	∣ – Copyright (C)) 2012 American Megatrends, Inc.
CPU Configuration		▲ Enabled for Windows XP and
Intel(R) Core(TM) i7-36120E CPU @	2.10GHz	Huper-Threading Technology)
CPU Signature	306a9	and Disabled for other OS (OS
Microcode Patch	17	not optimized for
Max CPU Speed	2100 MHz	Hyper-Threading Technology).
Min CPU Speed	1200 MHz	When Disabled only one thread
CPU Speed	2100 MHz	per enabled core is enabled.
Processor Cores	4	
Intel HT Technology	Supported	
Intel VI-X lechnology	Supported	
inter SMX rechnology	Supported	
04-b1(Supporteu	++· Select Screen
L1 Data Cache	32 kB x 4	11: Select Item
L1 Code Cache	32 KB X 4	Enter: Select
L2 Cache	256 kB x 4	+/-: Change Opt.
L3 Cache	6144 kB	F1: General Help
		F2: Previous Values
Hyper-threading	[Enabled]	F3: Optimized Defaults
Active Processor Cores	[A11]	F4: Save & Exit
Limit CPUID Maximum	[Disabled]	ESC: Exit
Execute Disable Bit	[Enabled]	
Intel Virtualization Technology	[Disabled]	
Haruware Pretetcher	[Fuspied]	•
Version 2.15.1236.	Copyright (C) 2	2012 American Megatrends, Inc.

Figure 2.6 CPU configuration

Hyper-Threading

This item allows you to enable or disable Intel? Hyper Threading technology. The default setting is "Enabled".

Active Processor Cores

This item allows you to configure the Processor Cores quantity from "1" to "All". The default setting for this item is set to "All".

Limit CPUID Maximum

This item allows you to enable or disable Limit CPUID Maximum. The default setting is "Disabled".

Execute Disable Bit

This item allows you to enable or disable the No-Execution page protection technology. The default setting for this item is set to "Enabled".

Intel virtualization technology

This item allows multiple operating systems to simultaneously share processor resources in a safe and efficient manner when this item is set to "Enabled".

The default setting is "Disabled".

Hardware Prefetcher

This item allows CPU to prefetch the instruction and data from memory to L2 Cache before CPU processing it. This will help system working more efficiently. The default setting for this item is set to "Enabled".

2.2.2.3 SATA Configuration

Aptio Setup L Advanced	Jtility – Copyright (C) 2012 Am∈	erican Megatrends, Inc.
SATA Controller(s) SATA Mode Selection SATA Controller Speed	[Enabled] [AHCI] [Default]	▲ Enable or disable SATA Device.
Serial HiH Port 0 Software Preserve Port 0 SATA Device Type Spin Up Device Serial ATA Port 1 Software Preserve Port 1 Hot Plug	Empty Unknown [Enabled] [Hard Disk Driver] [Disabled] Empty Unknown [Enabled] [Disabled]	
External SATA SATA Device Type Spin Up Device Serial ATA Port 2 Software Preserve Port 2 Hot Plug External SATA Spin Up Device Serial ATA Port 3	(Disabled) [Hard Disk Driver] [Disabled] Empty Unknown [Enabled] [Disabled] [Disabled] [Disabled] Empty	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Port 3 Version 2.15	[Enabled] 5.1236. Copyright (C) 2012 Ameri	▼ ican Megatrends, Inc.

Figure 2.7 SATA configuration

This option allows you to change the serial ATA port status. The port 5 is fixed for the optional on board SATA NAND Flash SSD. The default setting for each of this item is set to "Enabled".

SATA controller(s)

This option allows you to Enable or Disable the serial ATA device.

SATA Mode Selection

This option allows you to choose AHCI Mode or IDE Mode. The default setting is AHCI Mode. Windows XP OS is limited to IDE Mode, AHCI Mode is not supported under Windows XP.

SATA Controller Speed

This option allows you to choose the speed the SATA controller can support. "Default" means the the maximum speed the SATA controller can support.

Serial ATA Port 0~4

This option allows you to change the serial ATA port status. The "Serial ATA port 5" is fixed for the optional on board SATA NAND Flash SSD. The default setting for each of this item is set to "Enabled".

2.2.2.4 USB Configuration

Aptio Setup Utility — (Advanced	Copyright (C) 2012 American	Megatrends, Inc.
USB Configuration		Enables Legacy USB support.
USB Devices:) liuba	support if no USB devices are
i brive, i kegboard, i Mouse, .	o nuus	keep USB devices available
Legacy USB Support	[Enabled]	only for EFI applications.
USB3.0 Support	[Enabled]	
XHCI Hand-off	[Enabled]	
EHCI Hand-off	[Disabled]	
USB Mass Storage Driver Support	[Enabled]	
Port 60/64 Emulation	[Enabled]	
USB hardware delays and time-outs:		
USB transfer time-out	[20 sec]	++: Select Screen
Device reset time-out	[20 sec]	†↓: Select Item
Device power-up delay	[Auto]	Enter: Select
		+/−: Change Opt.
Mass Storage Devices:		F1: General Help
KingstonDataTraveler2.0 1.00	[Auto]	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Wersion 2 15 1236 Co	ouright (C) 2012 American M	eratrends Inc
VEI STOIT 2.13.1230. CO	Syr Ignit (C) 2012 Miller Itali Mi	eguti chus, inc.

Figure 2.8 USB configuration

USB Devices

This option allows you to check and change the USB device status.

- USB hardware delays and time-outs
 The recommended setting is as the picture above.
- Mass Storage Devices This option shows you the USB device which is connected.

2.2.2.5 H/W Monitor Configuration

Aptio Setup Ut Advanced	ility – Copyright (C) 2012 f	American Megatrends, Inc.
Pc Health Status CPU temperature System temperature VTT VCCSA +1.5V DDR3 +1.8V Vcore +5VSB +5V +3.3V +3.3VSB VBAT	: +59 C : +53 C : +0.996 V : +0.804 V : +1.510 V : +1.790 V : +0.822 V : +4.979 V : +4.979 V : +3.336 V : +3.324 V : +3.216 V	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.15.	1236. Copyright (C) 2012 Ame	erican Megatrends, Inc.

Figure 2.9 H/W Monitor configuration

System temperature, CPU temperature and Voltage status can be checked on Hardware monitor Configuration.

2.2.2.6 Super IO Configuration

Aptio Setup Utility - Advanced	Copyright (C) 2012 American	Megatrends, Inc.
Super IO Configuration		Set Parameters of Serial Port
Super IO Chip > Serial Port 0 Configuration > Serial Port 1 Configuration > Serial Port 2 Configuration > Serial Port 3 Configuration	SMSC SCH3106	• (COMA) • (COMA) • Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.15.1236. Co	pyright (C) 2012 American M	egatrends, Inc.

Figure 2.10 Super IO configuration

This option allows you to set parameters of each serial port.

2.2.2.7 Serial Port Console Redirection

Aptio Setup Utility — (Advanced	Copyright (C) 2012 American	Megatrends, Inc.
COM1 Console Redirection ▶ Console Redirection Settings	[Disabled]	Console Redirection Enable or Disable.
COM2 Console Redirection ▶ Console Redirection Settings	[Disabled]	
COM3 Console Redirection ▶ Console Redirection Settings	[Disabled]	
COM4 Console Redirection ▶ Console Redirection Settings	[Disabled]	++: Select Screen 14: Select Item Enter: Select +/-: Change Ont.
Serial Port for Out-of-Band Managemen Windows Emergency Management Service: Console Redirection ▶ Console Redirection Settings	nt∕ s (EMS) [Disabled]	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit
		ESC: Exit
Version 2.15.1236. Co	pyright (C) 2012 American M	egatrends, Inc.

Figure 2.11 Serial Port Console Redirection configuration

This option allows you to enable or disable the Console Redirection function. The default setting is "Disabled"

2.2.2.8 Network Stack

Aptio Set Advanced	up Utility – Copyright (C) 2012 Americ	an Megatrends, Inc.
Network stack	[Disabled]	Enable/Disable UEFI network stack ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version	2.15.1236. Copyright (C) 2012 American	Megatrends, Inc.

Figure 2.12 Network Stack configuration

This option allows you to enable or disable the Network Stack function. The default setting is "Disabled".

2.2.2.9 CPU PPM Configuration

Aptio Setup Utility - Advanced	– Copyright (C) 2012 Americ	an Megatrends, Inc.
CPU PPM Configuration		Enable/Disable Intel SpeedStep
EIST Turbo Mode CPU C3 Report CPU C6 report Config TDP LOCK Long duration power limit Long duration maintained Short duration power limit ACPI T State	[Enabled] [Enabled] [Enabled] [Enabled] [Disabled] 0 0 0 [Disabled]	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
version 2.15.1236.	copyright (ε) 2012 American	Megatrends, Inc.

Figure 2.13 CPU PPM configuration

This page shows the CPU status. Different CPU may show different information.

EIST

This option allows you to set the CPU SpeedStep function.

- Turbo Mode This option allows you to set the Turbo Mode function.
- CPU C3 ~ C7 Report

The option C3, C6, C7 allows you to set the power management function to save power.

2.2.3 Chipset Setup

2.2.3.1 Chipset Configuration

Aptio Setup Utility – Copyright (C) 2012 American Main Advanced <mark>Chipset</mark> Boot Security Save & Exit	Megatrends, Inc.
 PCH-IO Configuration System Agent (SA) Configuration 	PCH Parameters
	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.15.1236. Copyright (C) 2012 American Me	gatrends, Inc.

Figure 2.14 Chipset setup

2.2.3.2 PCH-IO Configuration

Aptio Setup U Chipset	tility – Copyright (C) 2012 Am	erican Megatrends, Inc.
Intel PCH RC Version Intel PCH SKU Name Intel PCH Rev ID > PCI Express Configuration > USB Configuration	1.8.0.1 QM77 04/C1	PCI Express Configuration settings
		++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.15	.1236. Copyright (C) 2012 Amer	ican Megatrends, Inc.



2.2.3.3 PCI Express Configuration

PCI Express Configuration		Enable or disable PCI Express Clock Gating for each root
PCI Express Clock Gating [DMI Link ASPM Control [DMI Link Extended Synch Control [Enabled] Enabled] Disabled]	port.
PCIe-USB Glitch W/A [Subtractive Decode [Disabled] Disabled]	
 PCI Express Root Port 1 PCI Express Root Port 2 PCI Express Root Port 3 		
 PCI Express Root Port 4 PCI Express Root Port 5 PCI Express Root Port 6 		++: Select Screen
 PCI Express Root Port 7 PCI Express Root Port 8 		fl: Select Item Enter: Select
		F1: General Help F2: Previous Values
		F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2 15 1296 Conu	right (C) 2012 American Ma	agatrends Inc

Figure 2.16 PCI Express configuration

This option allows you to Enable or Disable the PCIe clock gating for each root port.

Ap<u>tio Setup</u> Utility – Copyright (C) 2012 American Megatrends, Inc. Chipset USB Configuration Enable or disable XHCI Pre-Boot Driver support. xHCI Mode [Smart Auto] HS Port #1 Switchable [Enabled] HS Port #2 Switchable [Enabled] [Enabled] HS Port #3 Switchable HS Port #4 Switchable [Enabled] xHCI Streams [Enabled] EHCI1 [Enabled] EHC12 [Enabled] ↔: Select Screen USB Ports Per-Port Disable Control [Disabled] ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc

2.2.3.4 USB Configuration

Figure 2.17 USB configuration

XHCI Pre-Boot Driver

This option allows you to Enable or Disable the XHCI Pre-Boot Driver.

- xHCI Mode This option allows you to Enable or Disable the xHCI mode.
- HS Port #1~4 Switchable This option allows you to Enable switch function between xhci and ehci.
- xHCI Streams This option allows you to Enable or Disable the xHCI Streams.
- EHCI 1~2

This option allows you to Enable or Disable the switch for EHCI controller 1~2.

USB Ports Per-Port Disable Control

This option allows you to Enable or Disable the general control switch for USB Port.

2.2.3.5 System Agent Configuration

Aptio Setup Chipset	Utility – Copyright (C) 2012 f	American Megatrends, Inc.
System Agent Bridge Name System Agent RC Version VT–d Capability	IvyBridge 1.8.0.0 Supported	Check to enable VT-d function on MCH.
VT-d	[Enabled]	
 Graphics Configuration NB PCIe Configuration 		
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.1	5.1236. Copyright (C) 2012 Ame	erican Megatrends, Inc.

Figure 2.18 System Agent configuration

The option "VT-d" allows you to Enable or Disable the Intel virtualization for directed I/ O function.

2.2.3.6 Graphics configuration



Figure 2.19 Graphics configuration

This page shows the Graphic status and allows you to set the features.

2.2.3.7 NB PCIe configuration

Aptio Setup U Chipset	tility – Copyright (C) 2012 Ame	rican Megatrends, Inc.
NB PCIe Configuration PEGO PEGO – Gen X PEGO ASPM	Not Present [Auto] [Disabled]	Configure PEGO BO:D1:FO Gen1-Gen3
Enable PEG	[Auto]	
		<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.15	.1236. Copyright (C) 2012 Ameri	can Megatrends, Inc.

Figure 2.20 NB PCIe configuration

This option allows system automatically detect PCIe device generation.

2.2.4 Boot Setup

2.2.4.1 Boot Configuration



Figure 2.21 Boot setup

Setup Prompt Timeout

This option allows you to set the time before setup hotkey working.

Bootup NumLock State

This setting allows system automatically turns on your NumLock key when the system is booted. The default setting is "on".

Boot Option Priorities The option shows you the boot priority of device."Boot Option #1" has the first priority and then" Boot Option #2".

Hard Drive BBS Priorities

This option allows you to set the priority of device to boot.

2.2.4.2 CSM16 Parameters Settings Configuration



Figure 2.22 CSM16 Parameters setting

GateA20 Active

This option is useful when RT code is executed 1MB.GateA20 can be disabled using BIOS service in "Upon Request" setting. Do not allow disabling GateA20 in "Always" setting.

Option ROM Messages

This option allows you to set the display mode for Option ROM with"Force BIOS" or "Keep Current". The default setting is "Force BIOS".

INT19 Trap Response

This option allows you to choose "Immediate" execute the trap right away or choose "Postponed" to execute the trap during legacy boot.

2.2.5 Security Setup

Aptio Setup Utilit Main Advanced Chipset Boot	y – Copyright (C) 2012 American <mark>Security </mark> Save & Exit	Megatrends, Inc.
Password Description		Set Administrator Password
If ONLY the Administrator's pass then this only limits access to only asked for when entering Set If ONLY the User's password is s is a power on password and must boot or enter Setup. In Setup th have Administrator rights. The password length must be in the following range: Minimum length	word is set, Setup and is up. et, then this be entered to e User will 3	
Maxımum length	20	
Administrator Password User Password		Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.15.1236	. Copyright (C) 2012 American M	egatrends, Inc.

Figure 2.23 Password configuration

Select Security Setup from the MIC-3328 Setup main BIOS setup menu. Password protection is described in this section. To access the sub menu for the following items, select the item and press <Enter>:

Administrator Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the Administrator password.

User Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the User Password.

2.2.6 Save & Exit Option

Aptio Setup Utility – Copyright (C) 2012 American Main Advanced Chipset Boot Security <mark>Save & Exit</mark>	Megatrends, Inc.
Save Changes and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Save Changes Discard Changes Restore Defaults Save as User Defaults Restore User Defaults	Exit system setup after saving the changes.
Boot Override KingstonDataTraveler2.0 1.00 UEFI: KingstonDataTraveler2.0 1.00 Launch EFI Shell from filesystem device	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.15.1236. Copyright (C) 2012 American Me	egatrends, Inc.

Figure 2.24 Save and Exit configuration

2.2.6.1 Save Changes and Exit

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and when reboot the computer to take effect all system configuration parameters.

- 1. Select "Save Changes and Exit" and press <Enter>. The following message appears: Save Configuration and Exit? [Yes] [No]
- 2. Select Yes or No.

2.2.6.2 Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

- 1. Select "Discard Changes and Exit" and press <Enter>. The following message appears: Quit without saving? [Yes] [No]
- 2. Select Yes to discard changes and exit.

2.2.6.3 Save Changes and Reset

- 1. Select this option to save the changes and reboot the computer to take effect all system configuration parameters. Select this option the following message appears: Save Configuration and Reset? [Yes] [No]
- 2. Select Yes or No.

2.2.6.4 Discard Changes and Reset

- 1. Select "Discard Changes and Reset" and press <Enter>. The following message appears: Reset without saving? [Yes] [No]
- 2. Select Yes to discard changes and reset.

2.2.6.5 Save Options

Select this option to save or discard the changes

2.2.6.6 Restore Defaults

The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Save&Exit menu and press <Enter>.

2.2.6.7 Save as User Default

Save the all current settings as a user default.

2.2.6.8 Restore User Default

Restore all settings to user default values.

2.2.6.9 Boot Override

This option shows the boot device for you to choose.

MIC-3328 User Manual



Pin Assignments

This appendix describes pin assignments.

A.1 J1 Connector

Table A.1: J1 CompactPCI I/O						
PIN	Α	В	С	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD1	5V	V(I/O)	AD0	ACK64#	GND
23	3.3V	AD4	AD3	5V	AD2	GND
22	AD7	GND	3.3V	AD6	AD5	GND
21	3.3V	AD9	AD8	M66EN	CBE0	GND
20	AD12	GND	V(I/O)	AD11	AD10	GND
19	3.3V	AD15	AD14	GND	AD13	GND
18	SERR#	GND	3.3V	PAR	CBE1#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL#	PCIX_CAP	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12-14			KEY AR	EA		
11	AD18	AD17	AD16	GND	CBE2#	GND
10	AD21	GND	3.3V	AD20	AD19	GND
9	CBE3#	IDSEL	AD23	GND	AD22	GND
8	AD26	GND	V(I/O)	AD25	AD24	GND
7	AD30	AD29	AD28	GND	AD27	GND
6	REQ0#	GND	3.3V	CLK0	AD31	GND
5	NC	NC	RST#	GND	GNT0#	GND
4	NC	Healthy#	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	ТСК	5V	TMS	TDO	TDI	GND
1	5V	NC	TRST#	NC	5V	GND

Note!

NC: No Connect



#: Active Low

A.2 J2 Connector

Tab	le A.2: J2 Con	npactPCI I/O				
PIN	Α	В	С	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	NC	LAN1_MDIA 3+	LAN1_MDIA 1+	GND
20	CLK5	GND	NC	LAN1_MDIA 3-	LAN1_MDIA 1-	GND
19	GND	GND	NC	LAN1_MDIA 2+	LAN1_MDIA 0+	GND
18	NC	NC	NC	LAN1_MDIA 2-	LAN1_MDIA 0-	GND
17	RIO_PLTRST#	NC	PRST#	REQ6#	GNT6#	GND
16	PCIE_CLK_4-	PCIE_CLK_2+	DEG#	GND	5V	GND
15	PCIE_CLK_4+	PCIE_CLK_2-	FAL#	REQ5#	GNT5#	GND
14	PCIE_CLK_3-	PCIE_CLK_1+	PCIE_CLKRQ 4#	NC	5V	GND
13	PCIE_CLK_3+	PCIE_CLK_1-	PCIE_CLKRQ 3#	NC	NC	GND
12	PCIE1X4_RX+	PCIE_CLKRQ1 #	PCIE_CLKRQ 2#	NC	SATA3_Rx+	GND
11	PCIE1X4_RX-	PCIE1X4_TX+	USB4_P+	SATA3_Tx+	SATA3_Rx-	GND
10	PCIE1X3_RX+	PCIE1X4_TX-	USB4_P-	SATA3_Tx-	SATA2_Rx+	GND
9	PCIE1X3_RX-	PCIE1X3_TX+	USB3_P+	SATA2_Tx+	SATA2_Rx-	GND
8	PCIE1X2_RX+	PCIE1X3_TX-	USB3_P-	SATA2_Tx-	SATA1_Rx+	GND
7	PCIE1X2_RX-	PCIE1X2_TX+	USB2_P+	SATA1_Tx+	SATA1_Rx-	GND
6	PCIE1X1_RX+	PCIE1X2_TX-	USB2_P-	SATA1_Tx-	NC	GND
5	PCIE1X1_RX-	PCIE1X1_TX+	USB1_P+	NC	NC	GND
4	CPCI_VIO	PCIE1X1_TX-	USB1_P-	NC	GPIO	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note! NC: No Connect

#: Active Low

A.3 Other Connectors

Table A.3: XTM Board Connector (CN1, CN4, CN8, CN9)

Description	PIN	Description
PCIE16X_TX7+	2	PCIE16X_RX7+
PCIE16X_TX7-	4	PCIE16X_RX7-
GND	6	GND
CLK_XMC_GND+	8	PCIE16X_RX8+
CLK_XMC_GND-	10	PCIE16X_RX8-
GND	12	GND
PCIE16X_TX8+	14	PCIE_WAKE#
PCIE16X_TX8-	16	XMC_MPRESENT#
GND	18	XMC_SDA_SFP0
CLK_PEG_B+	20	XMC_SCL_SFP0
CLK_PEG_B-	22	SML1_CLK
GND	24	SML1_DATA
USB9_P-	26	USB_OC#1
USB9_P+	28	USB_OC#4
GND	30	SUS_CLK
USB8_P-	32	+VBAT
USB8_P+	34	+1.05V
GND	36	GPIO_8HP
VCC5	38	VCC3
VCC5	40	VCC3
	Description PCIE16X_TX7+ PCIE16X_TX7- GND CLK_XMC_GND+ CLK_XMC_GND- GND PCIE16X_TX8+ PCIE16X_TX8+ PCIE16X_TX8- GND CLK_PEG_B+ CLK_PEG_B- GND USB9_P- USB9_P+ GND USB8_P- USB8_P+ GND VCC5 VCC5	Description PIN PCIE16X_TX7+ 2 PCIE16X_TX7- 4 GND 6 CLK_XMC_GND+ 8 CLK_XMC_GND- 10 GND 12 PCIE16X_TX8+ 14 PCIE16X_TX8+ 16 GND 18 CLK_PEG_B+ 20 CLK_PEG_B- 22 GND 24 USB9_P- 26 USB9_P+ 28 GND 30 USB8_P- 32 USB8_P+ 34 GND 36 VCC5 38

CN4

PIN	Description	PIN	Description	
1	SATA0_RX+	2	AZ_BITCLK	
3	SATA0_RX-	4	AZ_SYNC	
5	GND	6	SPKR	
7	SATA0_TX+	8	AZ_RST#	
9	SATA0_RX-	10	AZ_SDIN0	
11	GND	12	AZ_SDOUT	
13	SATA4_RX+	14	XTM RESET	
15	SATA4_RX-	16	LAD0	
17	GND	18	LAD1	
19	SATA4_TX+	20	LAD2	
21	SATA4_TX-	22	LAD3	
23	GND	24	LFRAME#	
25	USB2_P-	26	LDRQ#0	
27	USB2_P+	28	SERIRQ	
29	GND	30	CLK33M_LPC	
31	USB3_P-	32	BUF_PLTRST#	
33	USB3_P+	34	KB_A20GATE	

35	GND	36	KB_RST#
37	VCC5	38	VCC3
39	VCC5	40	VCC3

CN8

CN9

PIN	Description	PIN	Description	
1	PCIE16X_TX0-	2	PCIE16X_RX1-	
3	PCIE16X_TX0+	4	PCIE16X_RX1+	
5	GND	6	GND	
7	PCIE16X_TX2+	8	PCIE16X_RX4-	
9	PCIE16X_TX2-	10	PCIE16X_RX4+	
11	GND	12	GND	
13	PCIE16X_TX1+	14	PCIE16X_RX6-	
15	PCIE16X_TX1-	16	PCIE16X_RX6+	
17	GND	18	GND	
19	PCIE16X_TX3-	20	PCIE16X_RX5+	
21	PCIE16X_TX3+	22	PCIE16X_RX5-	
23	GND	24	GND	
25	PCIE16X_TX5+	26	PCIE16X_RX3+	
27	PCIE16X_TX5-	28	PCIE16X_RX3-	
29	GND	30	GND	
31	PCIE16X_TX4-	32	PCIE16X_RX2-	

33	PCIE16X_TX4+	34	PCIE16X_RX2+
35	GND	36	GND
37	PCIE16X_TX6-	38	PCIE16X_RX0+
39	PCIE16X_TX6+	40	PCIE16X_RX0-

Table A.4: XMC Connector

PIN	Α	В	С	D	E	F
1	PCIE16X_R X0+	PCIE16X_R X0-	VCC3	PCIE16X_R X1+	PCIE16X_R X1-	VCC5
2	GND	GND	NC	GND	GND	XMC_RST#
3	PCIE16X_R X2+	PCIE16X_R X2-	VCC3	PCIE16X_R X3+	PCIE16X_R X3-	VCC5
4	GND	GND	NC	GND	GND	NC
5	PCIE16X_R X4+	PCIE16X_R X4-	VCC3	PCIE16X_R X5+	PCIE16X_R X5-	VCC5
6	GND	GND	NC	GND	GND	12V
7	PCIE16X_R X6+	PCIE16X_R X6-	VCC3	PCIE16X_R X7+	PCIE16X_R X7-	VCC5
8	GND	GND	NC	GND	GND	12V
9	NC	NC	NC	NC	NC	VCC5
10	GND	GND	NC	GND	GND	XMC_GA0
11	PCIE16X_TX 0+	PCIE16X_T X0-	NC	PCIE16X_T X1+	PCIE16X_T X1-	VCC5
12	GND	GND	XMC_GA1	GND	GND	XMC_MPRES ENT#
13	PCIE16X_TX 2+	PCIE16X_T X2-	NC	PCIE16X_T X3+	PCIE16X_T X3-	VCC5
14	GND	GND	XMC_GA2	GND	GND	XMC_SDA_S FP0
15	PCIE16X_TX 4+	PCIE16X_T X4-	NC	PCIE16X_T X5+	PCIE16X_T X5-	VCC5
16	GND	GND	NC	GND	GND	XMC_SCL_SF P0
17	PCIE16X_TX 6+	PCIE16X_T X6-	NC	PCIE16X_T X7+	PCIE16X_T X7-	NC
18	GND	GND	NC	GND	GND	NC
19	CLK_XMC_ GND+	CLK_XMC_ GND-	NC	XMC_WAKE #	XMC_ROO T0#	NC



Figure A.1 RJ45 LAN Indicator



CPLD

This appendix describes CPLD configuration.

B.1 Features

- **Hot-Swap:** Hot insertion and removal control
- CompactPCI Backplane: CompactPCI slot Addressing
- LPC Bus: Provide LPC Bus access
- Watchdog: Generates a reset signal or interrupt signal when timer overflows
- Debug Message: Boot time POST message

B.2 CPLD Introduction

Advantech MIC-3328 CPLD incorporates a LPC Unit to interconnect with a controller hub of an Intel south bridge (QM77). The LPC Unit translates the LPC interface signals to MIC-3328 CPLD internal local bus. The CPLD Internal Local Bus is used to control and communicate with I/O space. The I/O space includes a Watch Dog unit, a debug port unit, and a cPCI slot addressing unit. In addition, there is a Hot-Swap Out-Of-Service LED control unit.

B.3 Watchdog Timer

To program the watchdog timer, you must write a program which writes a value to I/O port address 443 (hex). Any non-zero value in I/O port 443h enables the watchdog function. The watchdog reset time is 1 ~ 255 seconds (1 second per step). Reading I/O port 444h will disable the watchdog. The return value is meaningless.



Glossary

C.1 Glossary

CPU	Central Processing Unit
CPCI	CompactPCI
CPLD	Complex Programmable Logic Device
EMC	Electro Magnetic Compatibiltiy
ESD	Electro Static Discharge
HDD	Hard Disk Drive
HW	HardWare
I/O	Input/Output
IC	Integrated Circuit
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
MAC	Medium Access Control
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCle	Peripheral Component Interconnect Express
PHY	Physical layer Interface
PMC	PCI interface mezzanine card
RIO	Rear Input/Output
RS-232	An Interface specified by Electronic Industries Alliance
RTC	Real Time Clock
RTM	Rear Transition Module
SBC	Single Board Computer
SDRAM	Synchronous DRAM
SPI	Serial Peripheral Interface
SSD	Solid State Disk
SW	SoftWare
XMC	PCIe interface mezzanine card
XTM	Extension Module



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